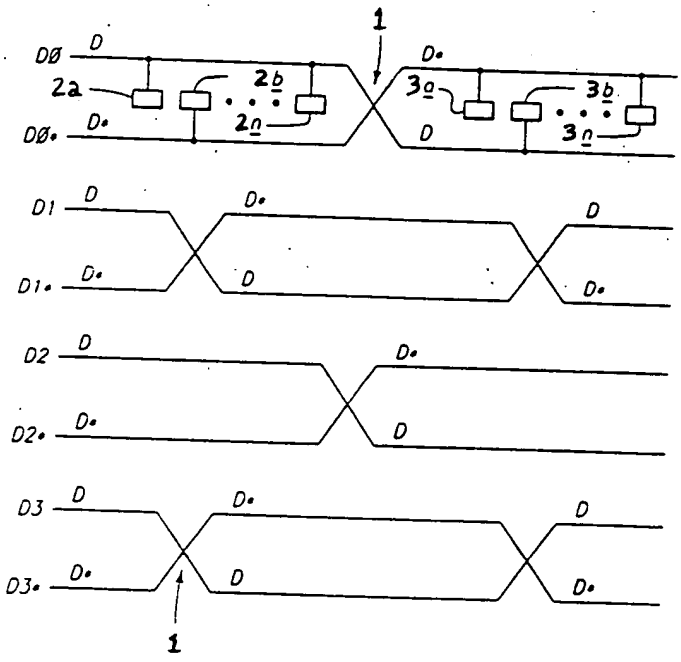


Fig 1
PRIOR ART

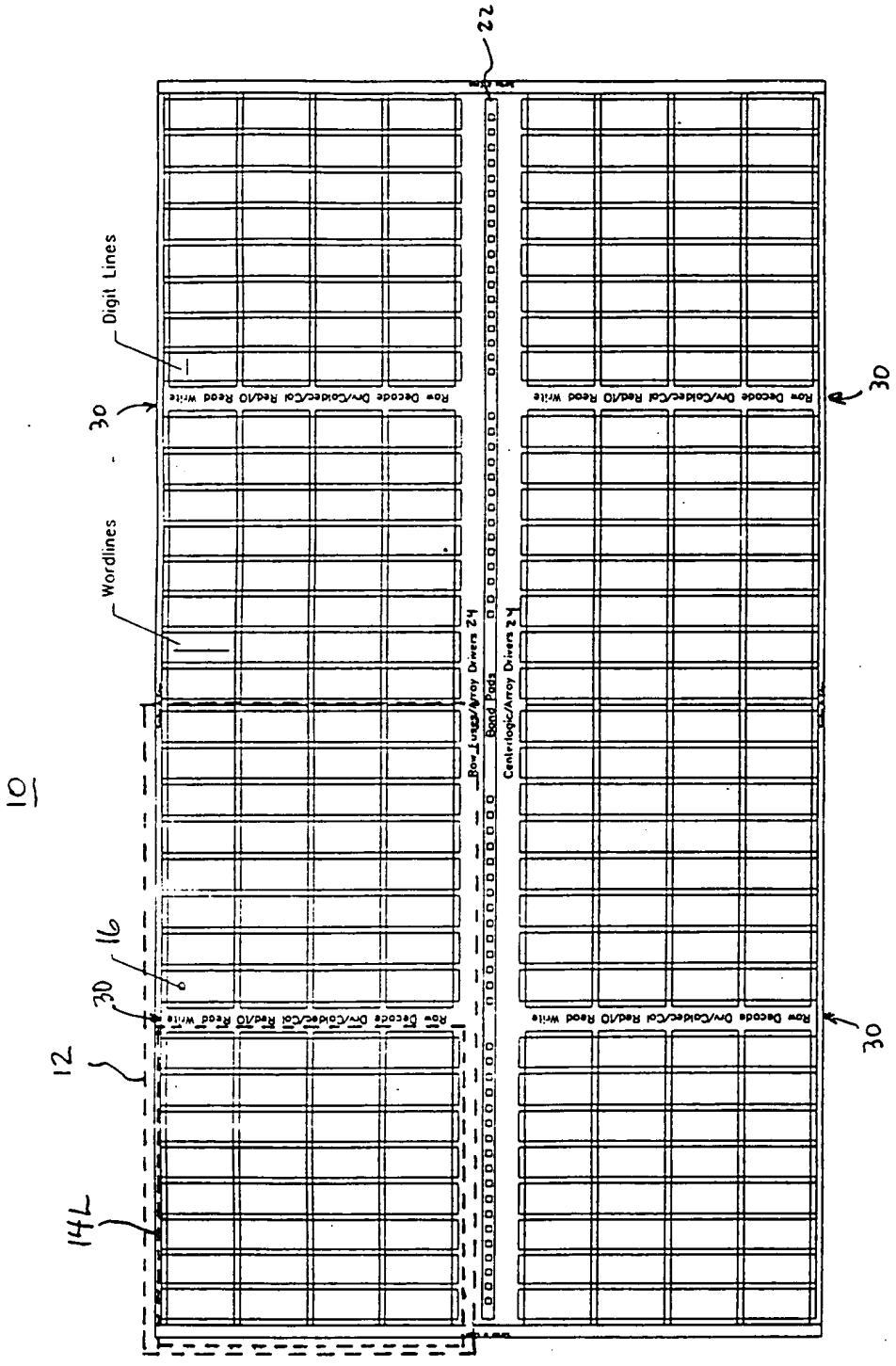

10
12
14
16
22
24
30
Digit Lines
Wordlines
Row Decode Drv/Coldec/Col Rd/Wr Read Write
Bond Pads
Centrilogic/Array Drivers

FIGURE 2

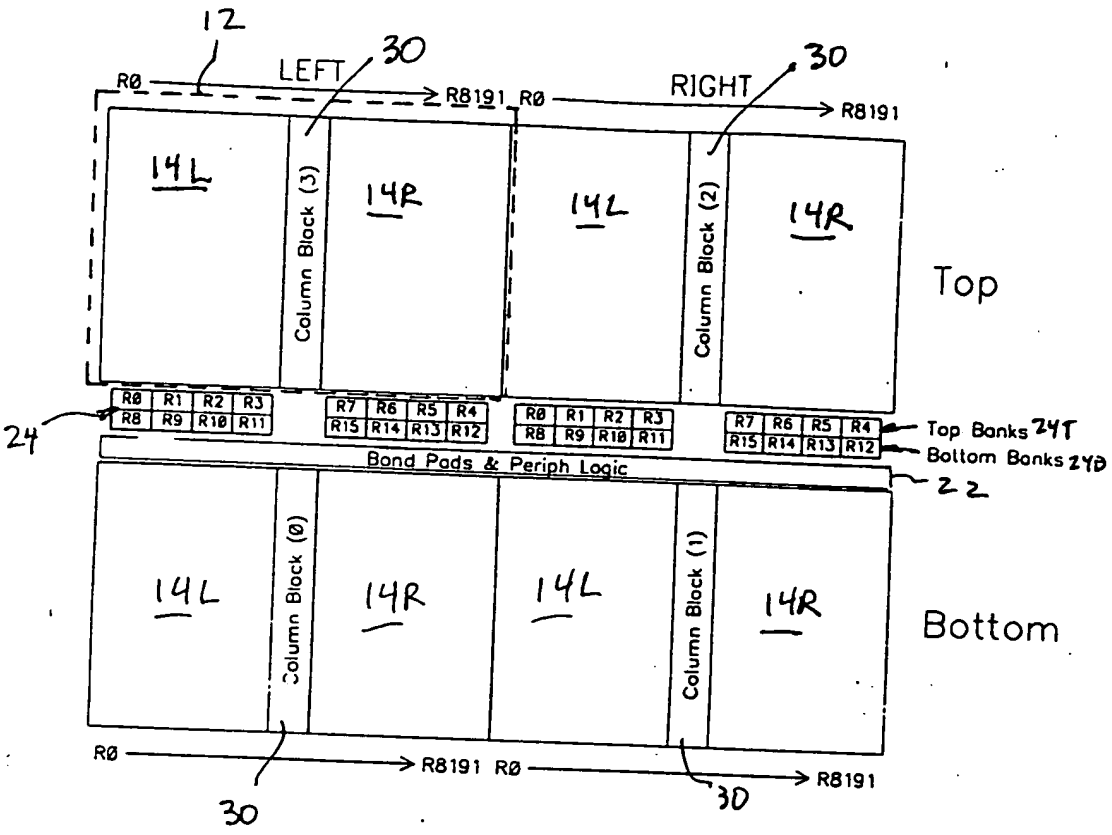


FIGURE 3

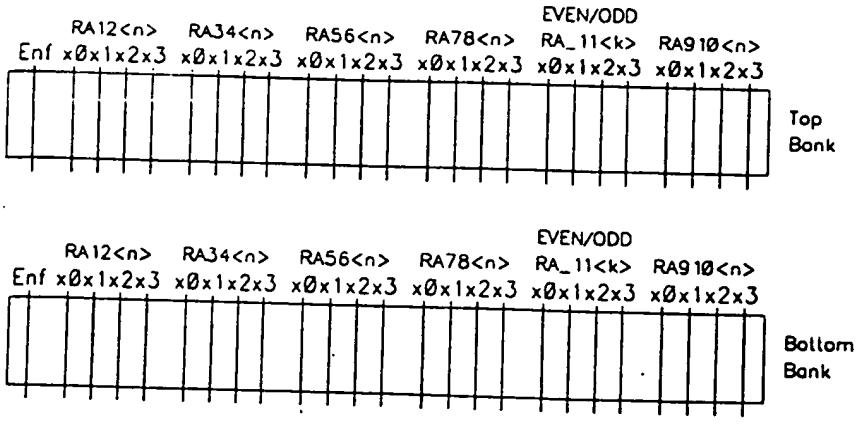


FIGURE 4

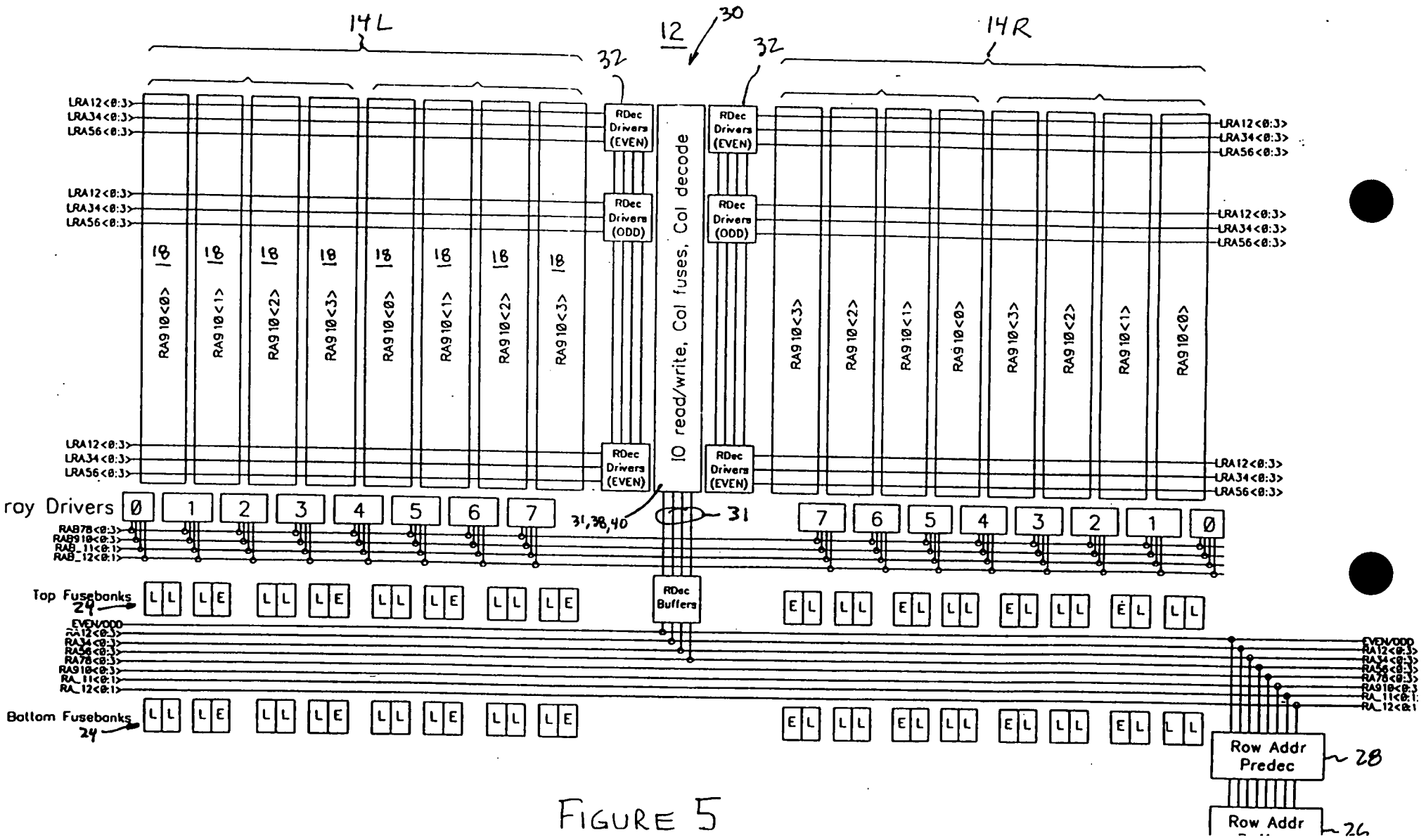

14L
12
30
32
32
14R
LRA12<0:3>
LRA34<0:3>
LRA56<0:3>
RDec Drivers (EVEN)
RDec Drivers (ODD)
IO read/write, Col fuses, Col decode
18
RA9 10<0>
RA9 10<1>
RA9 10<2>
RA9 10<3>
ray Drivers
0
1
2
3
4
5
6
7
31,38,40
31
RDec Buffers
Top Fusebanks
24
Bottom Fusebanks
24
EVEN/ODD
Row Addr Predec
28
Row Addr
26

FIGURE 5

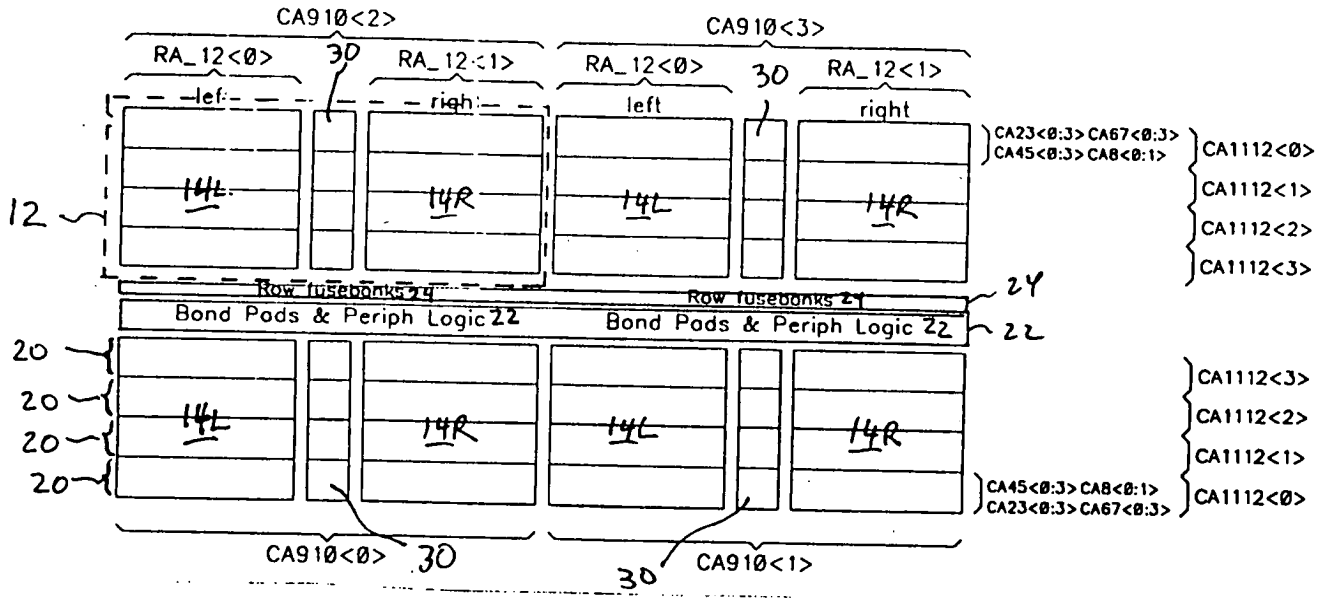

CA910<2>
CA910<3>
RA_12<0>
RA_12<1>
RA_12<0>
RA_12<1>
30
30
left
right
left
right
12
14L
14R
14L
14R
CA23<0:3> CA67<0:3>
CA45<0:3> CA8<0:1>
CA1112<0>
CA1112<1>
CA1112<2>
CA1112<3>
Row fusebanks 24
Row fusebanks 24
24
Bond Pads & Periph Logic 22
Bond Pads & Periph Logic 22
22
20
20
20
20
14L
14R
14L
14R
CA1112<3>
CA1112<2>
CA1112<1>
CA1112<0>
CA45<0:3> CA8<0:1>
CA23<0:3> CA67<0:3>
CA910<0>
30
30
CA910<1>

FIGURE 6

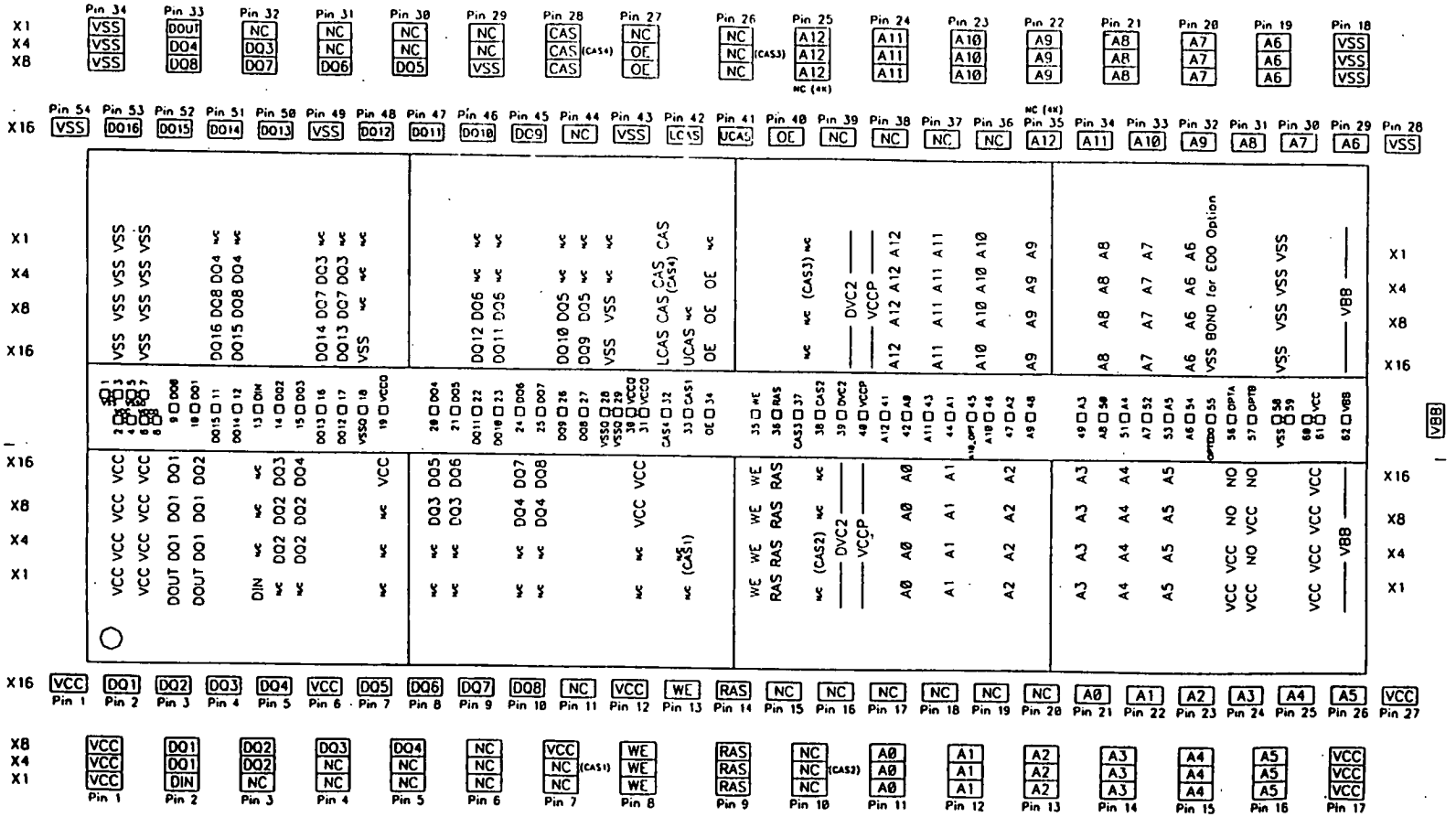


FIGURE 7

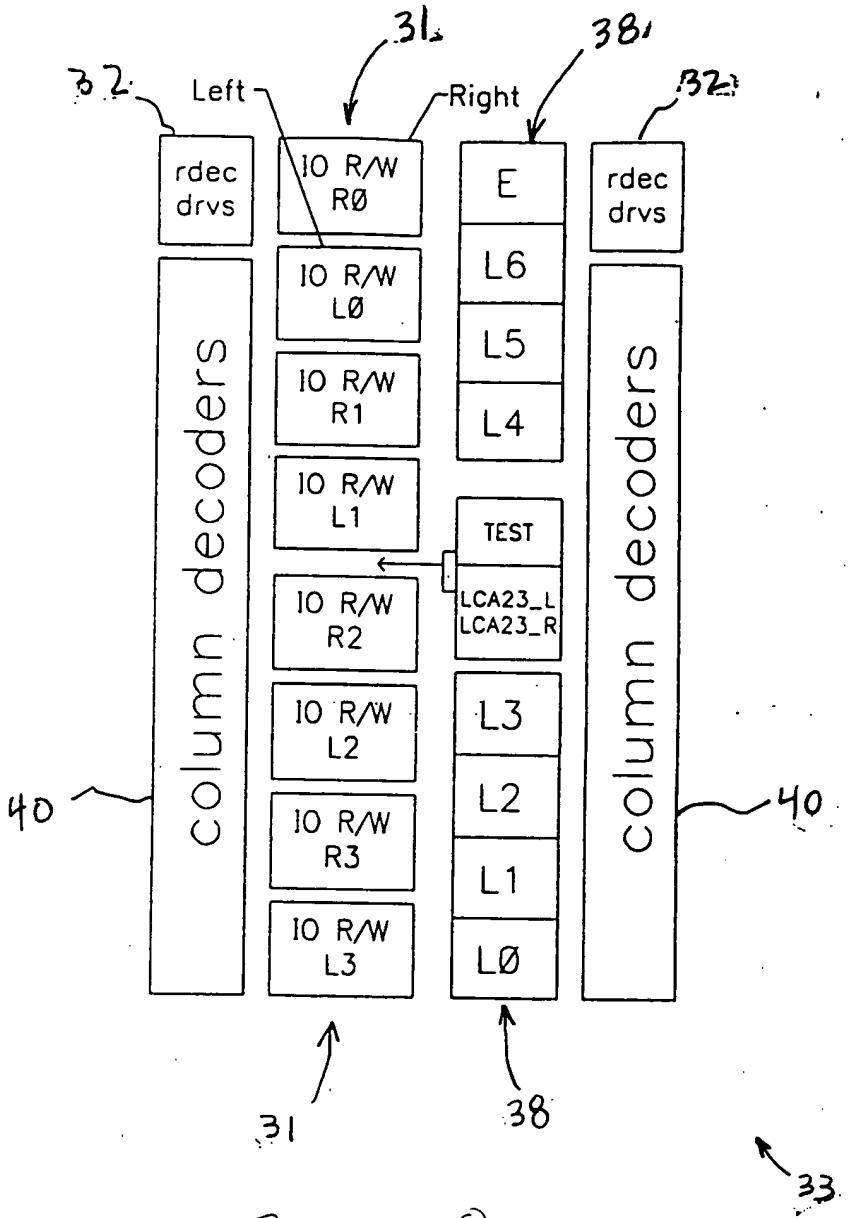


FIGURE 8

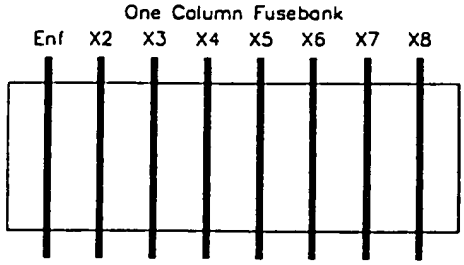


FIGURE 10

Row Redundant Laser Fuses

Row Predec Addr	Blow Laser Fuse			
RA12<0>	[x0]	x1	x2	x3
RA12<1>	x0	[x1]	x2	x3
RA12<2>	x0	x1	[x2]	x3
RA12<3>	x0	x1	x2	[x3]
RA34<0>	[x0]	x1	x2	x3
RA34<1>	x0	[x1]	x2	x3
RA34<2>	x0	x1	[x2]	x3
RA34<3>	x0	x1	x2	[x3]
RA56<0>	[x0]	x1	x2	x3
RA56<1>	x0	[x1]	x2	x3
RA56<2>	x0	x1	[x2]	x3
RA56<3>	x0	x1	x2	[x3]
RA78<0>	[x0]	x1	x2	x3
RA78<1>	x0	[x1]	x2	x3
RA78<2>	x0	x1	[x2]	x3
RA78<3>	x0	x1	x2	[x3]
EVEN	[x0]	x1	x2	x3
ODD	x0	[x1]	x2	x3
RA_11<0>	x0	x1	[x2]	x3
RA_11<1>	x0	x1	x2	[x3]
RA910<0>	[x0]	x1	x2	x3
RA910<1>	x0	[x1]	x2	x3
RA910<2>	x0	x1	[x2]	x3
RA910<3>	x0	x1	x2	[x3]

Note: Boxed fuses are the 'blown' fuses.

Pretest Address
(compressed to 8meg block; unscrambled addresses)

BLOCK		ROW Addresses
R0	R8	4,5,6,7
R1	R9	1016,1017,1018,1019
R2	R10	1028,1029,1030,1031
R3	R11	2040,2041,2042,2043
R4	R12	2052,2053,2054,2055
R5	R13	3064,3065,3066,3067
R6	R14	3076,3077,3078,3079
R7	R15	4088,4089,4090,4091

FIGURE 11

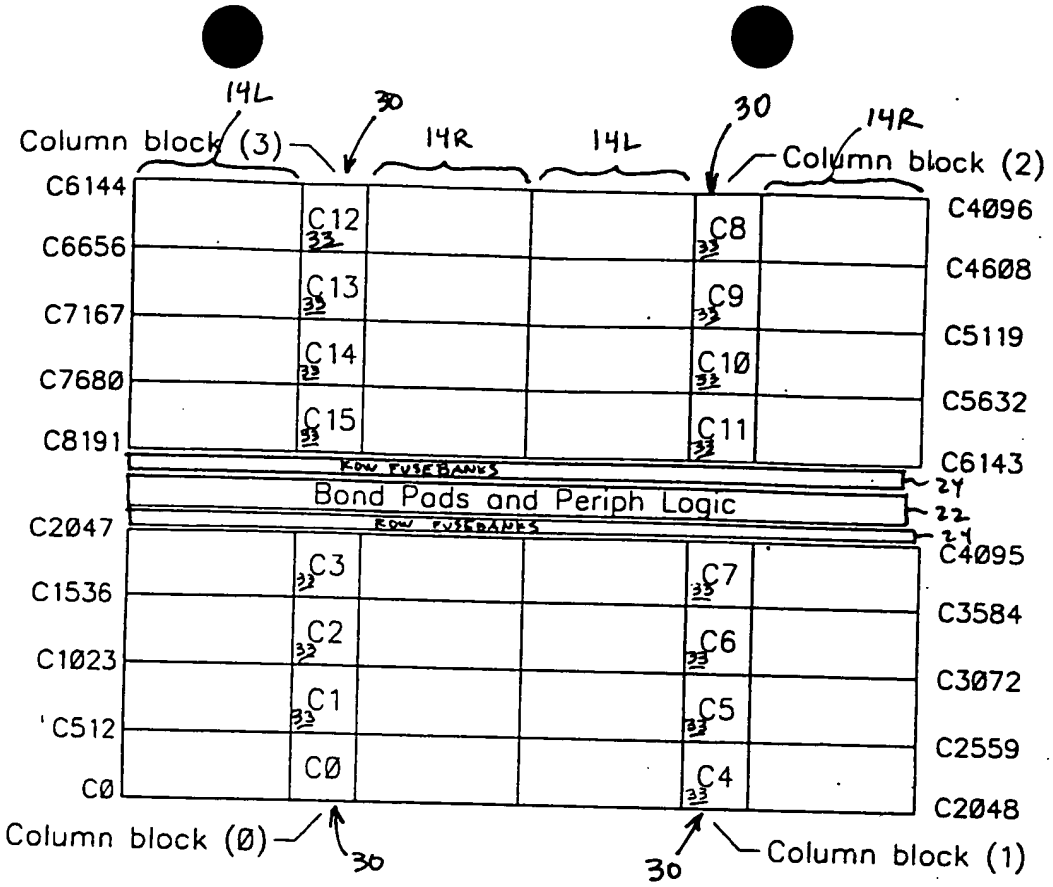


FIGURE 9

Column Redundant Laser Fuses

Col Predec Addr	Blow Laser Fuse
CA23<0>	NONE
CA23<1>	X2
CA23<2>	X3
CA23<3>	X2, X3
CA45<0>	NONE
CA45<1>	X4
CA45<2>	X5
CA45<3>	X4, X5
CA67<0>	NONE
CA67<1>	X6
CA67<2>	X7
CA67<3>	X6, X7
CA8<0>	NONE
CA8<1>	X8

Bank	Pre-test Address						
	A8	A7	A6	A5	A4	A3	A2
0	0	0	0	0	1	1	1
1	0	0	0	0	1	1	0
2	0	0	0	0	1	0	1
3	0	0	0	0	1	0	0
4	0	0	0	0	0	0	0
5	0	0	0	0	0	0	1
6	0	0	0	0	0	1	0
7	NA						

FIGURE 12

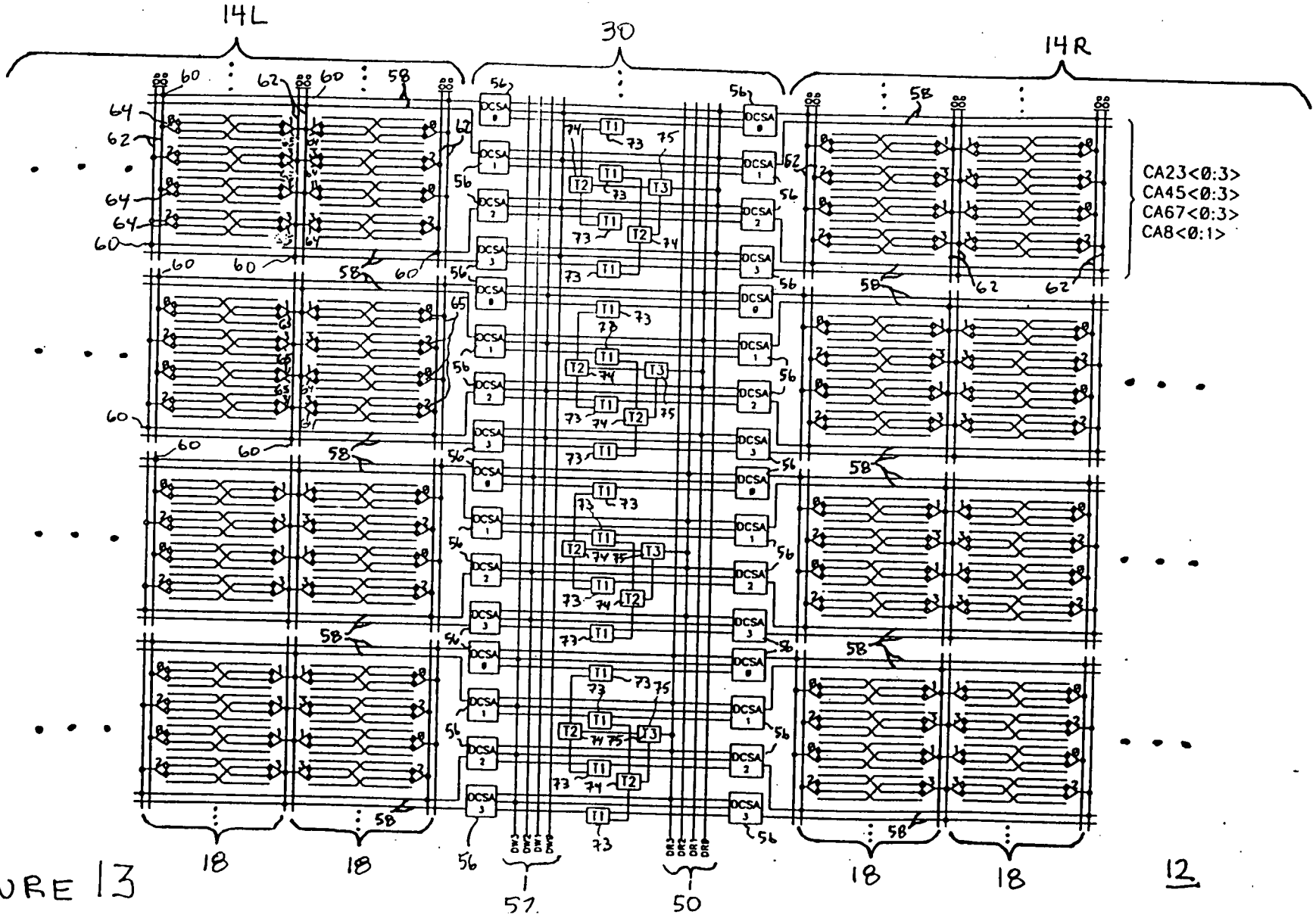


FIGURE 13

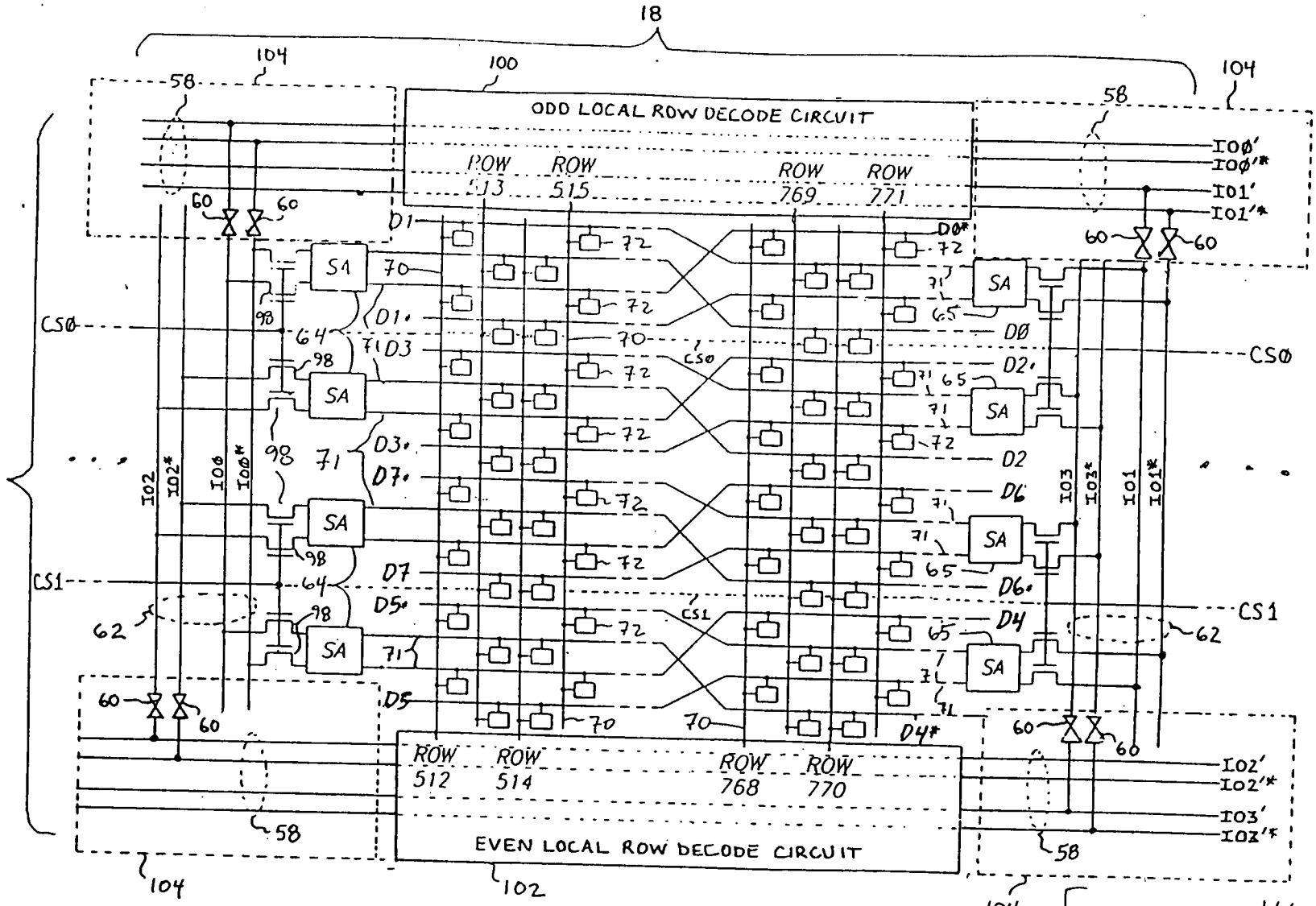

18
104
100
58
ODD LOCAL ROW DECODE CIRCUIT
ROW 513
ROW 515
ROW 769
ROW 771
IOØ'
IOØ'*
IO1'
IO1'*
60
SA
70
72
71
65
98
64
CSØ
CS1
D1
D3
D5
D7
DØ
D2
D4
D6
IO2
IO2*
IOØ
IOØ*
IO3
IO3*
IO1
IO1*
62
ROW 512
ROW 514
ROW 768
ROW 770
EVEN LOCAL ROW DECODE CIRCUIT
IO2'
IO2'*
IO3'
IO3'*
102

FIGURE 14

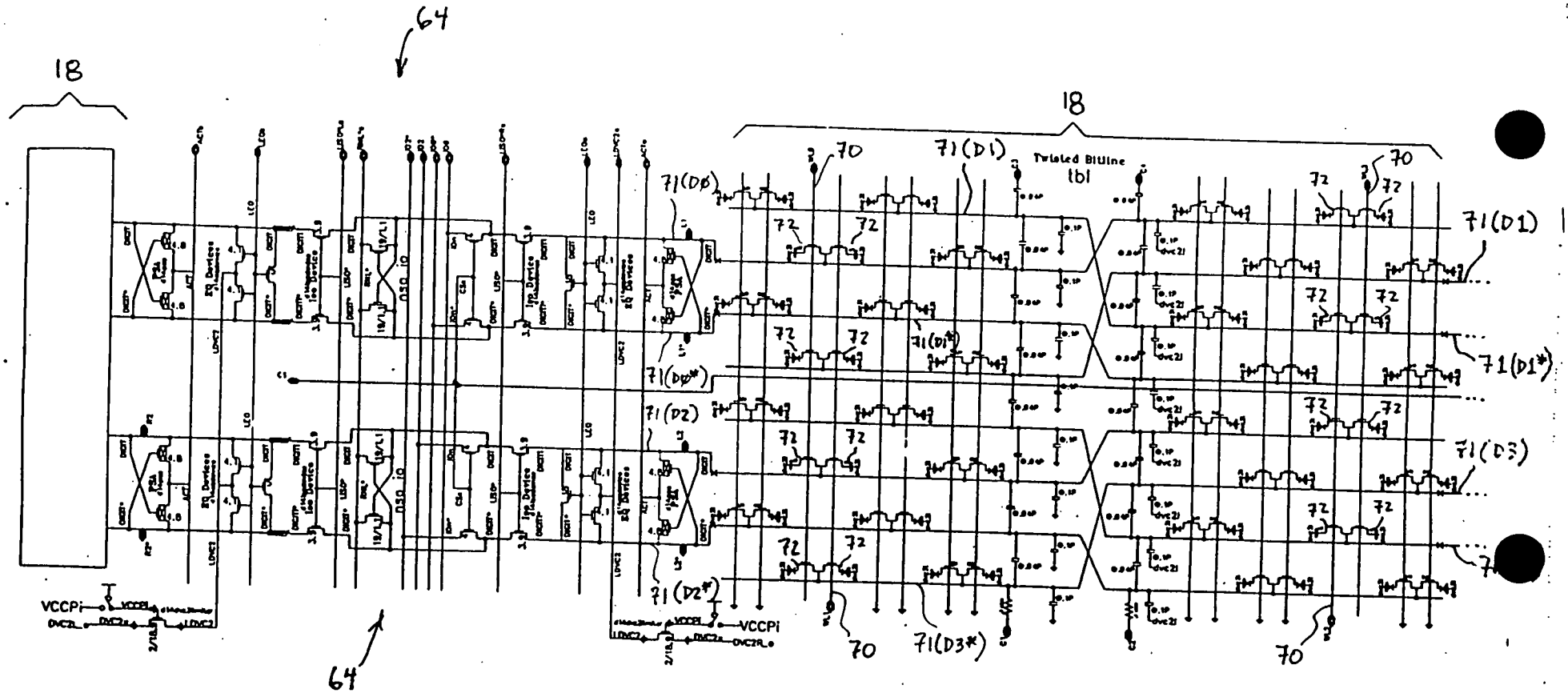
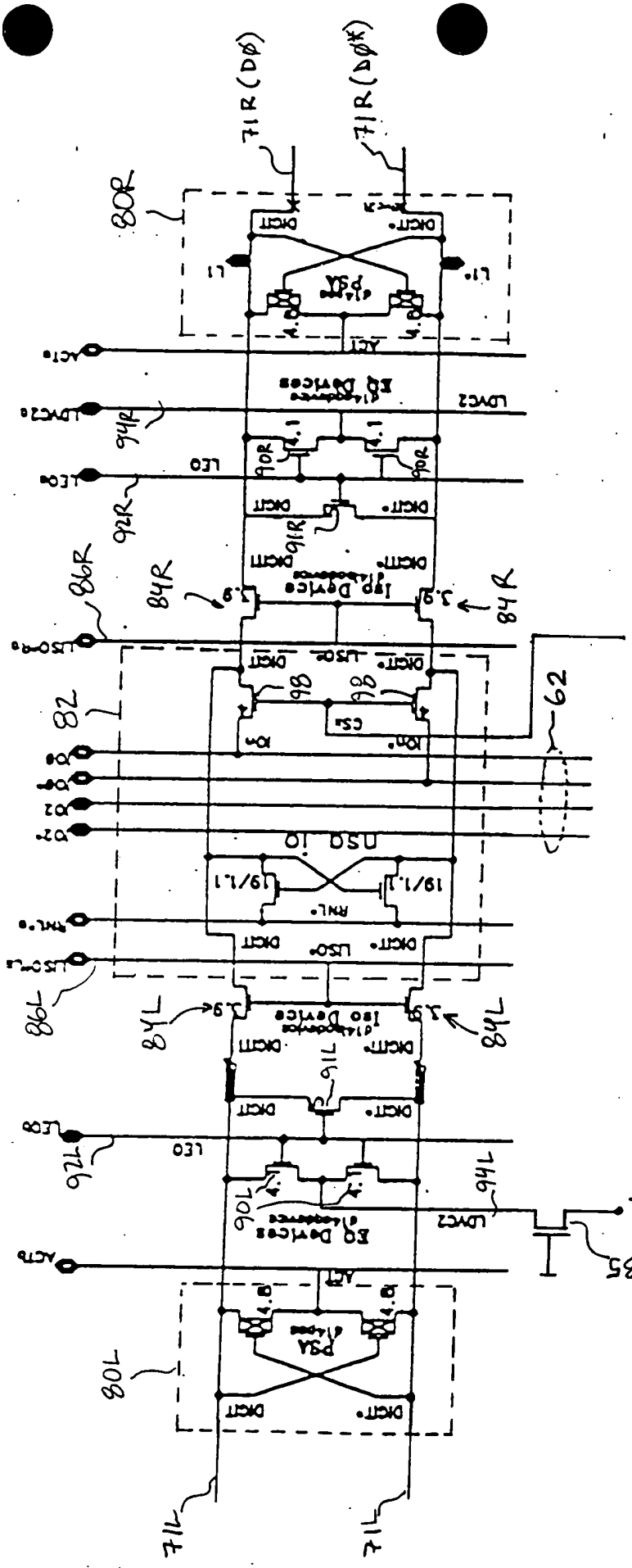

18
64
18
70
71(D1)
Twisted Bitline
tbl
71(D0)
72
71(D0*)
71(D1*)
71(D2)
71(D3)
71(D2*)
71(D3*)
VCCPi
64

FIGURE 15



64

FIGURE 16

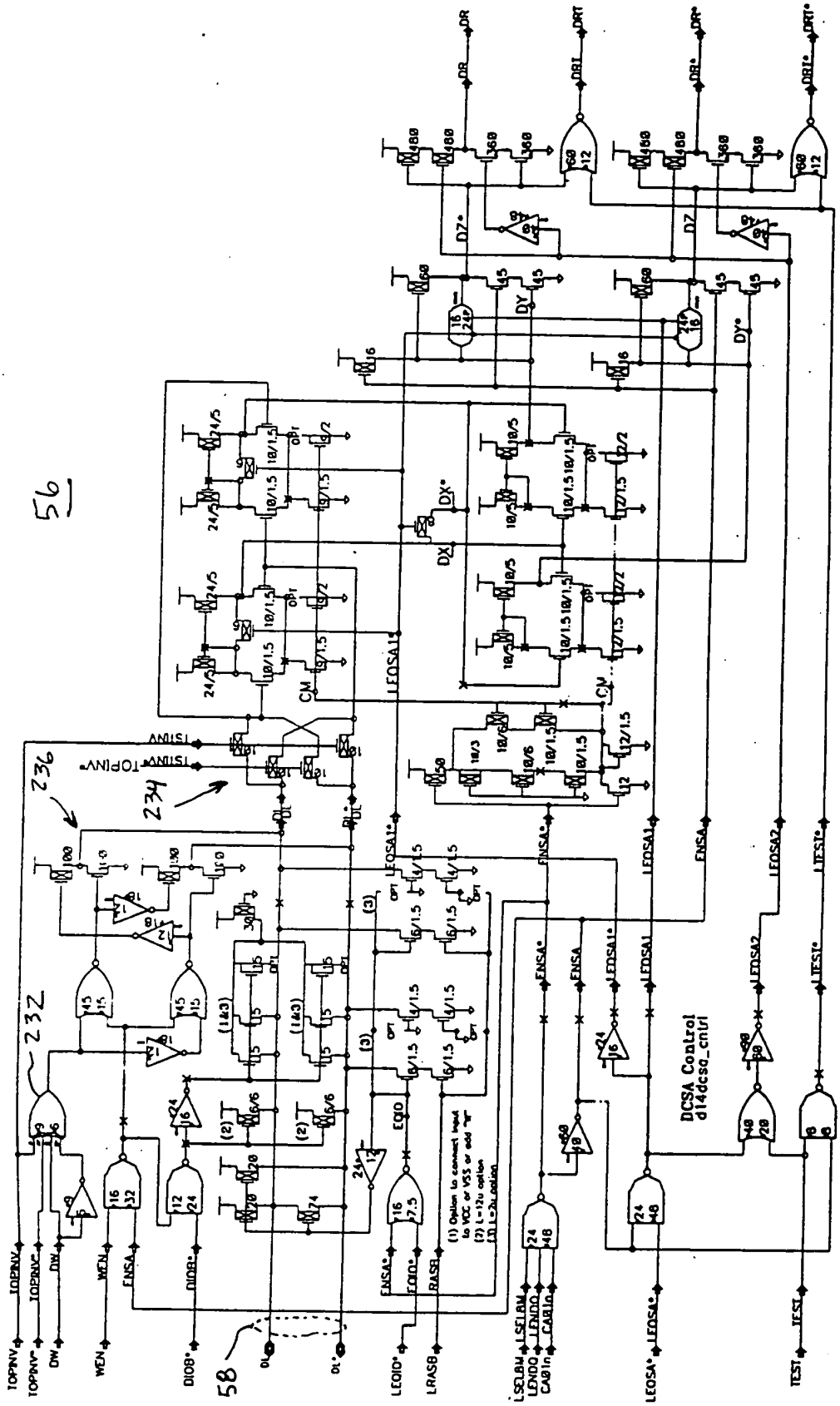

56
58
232
234
236
DCSA Control
d14dcsa_cntrl
(1) Option to connect input to VCC or VSS or add "R"
(2) L=12u option
(3) L=2u option

FIGURE 17

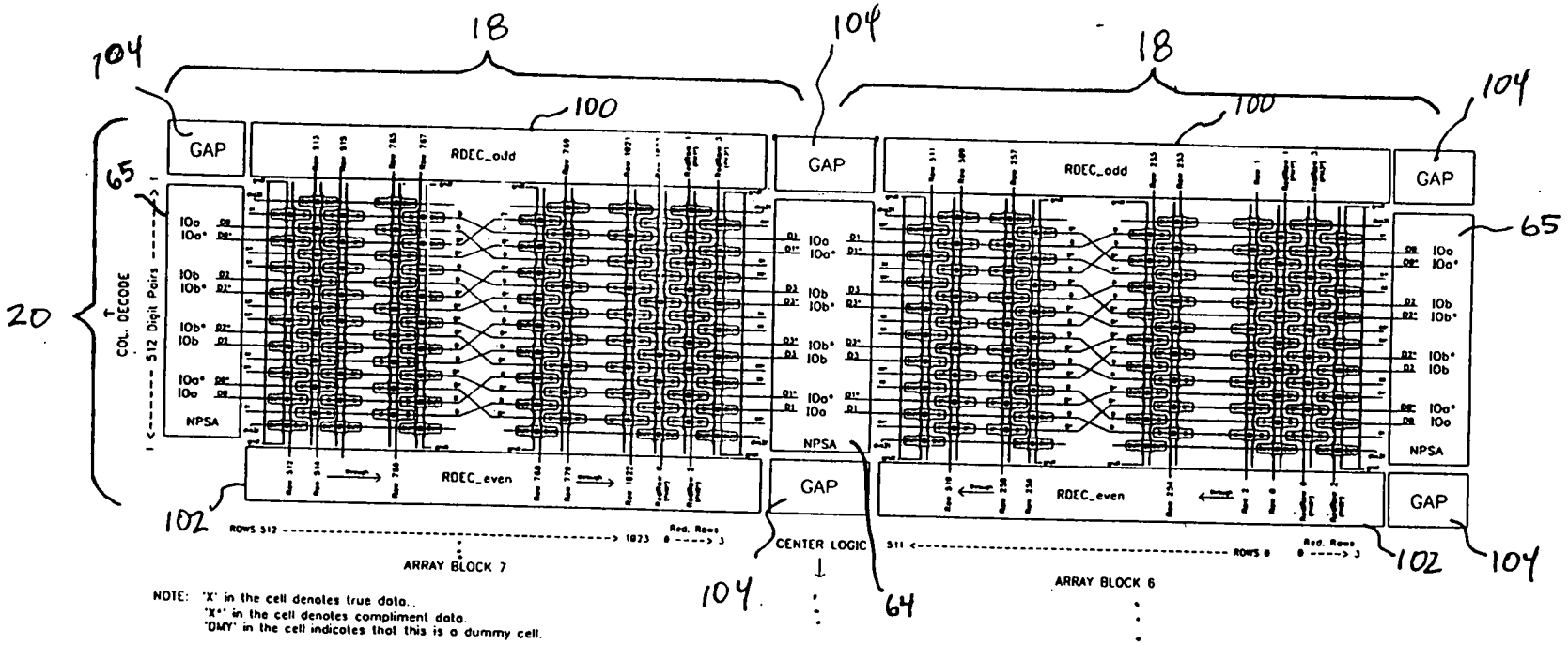

18
104
100
GAP
RDEC_odd
RDEC_even
NPSA
65
20
COL. DECODE
512 Digit Pairs
102
ROWS 512
1023
Red. Rows
ARRAY BLOCK 7
CENTER LOGIC
64
ROWS 0
511
ARRAY BLOCK 6
NOTE: 'X' in the cell denotes true data..
'X*' in the cell denotes compliment data.
'DMY' in the cell indicates that this is a dummy cell.

FIGURE 18

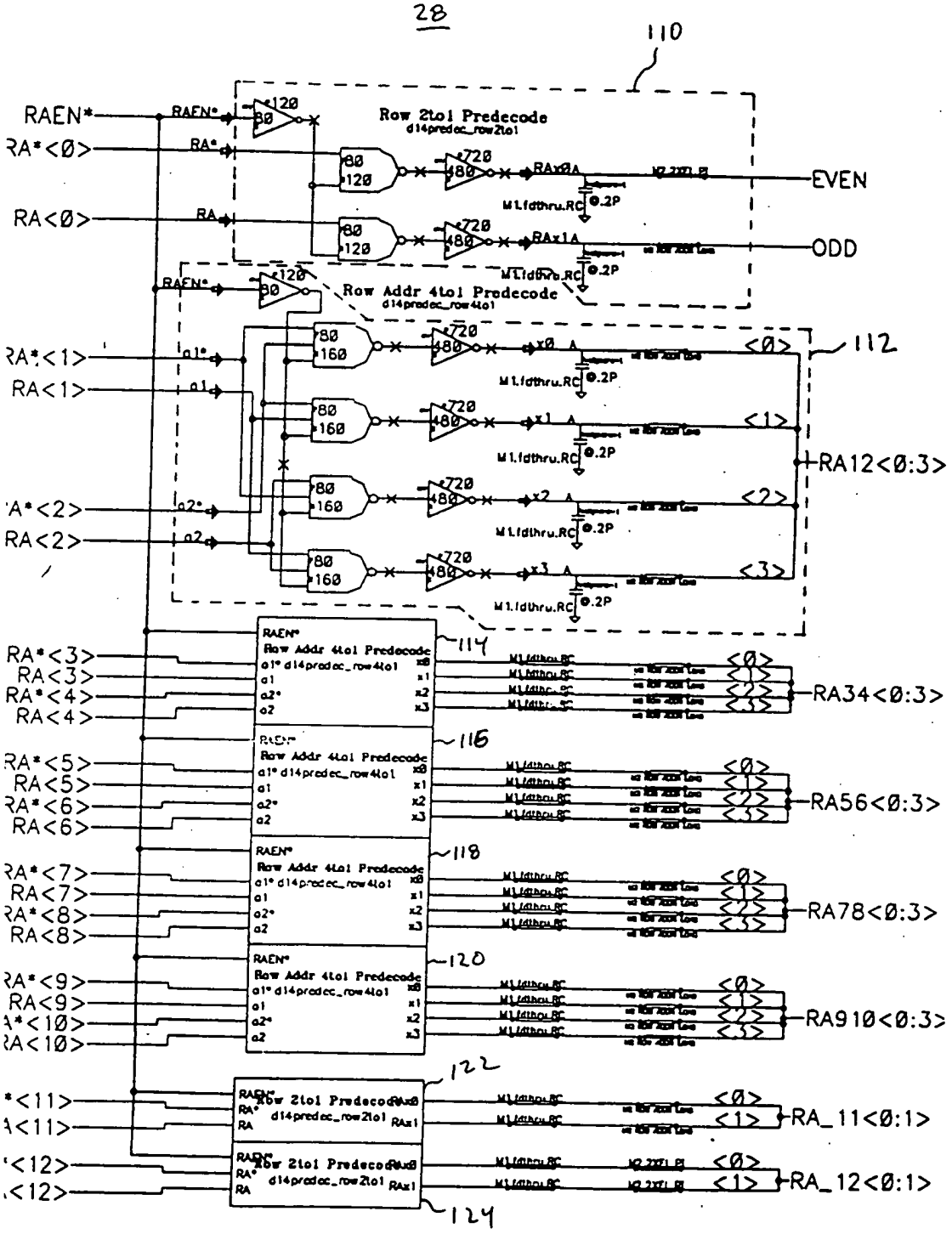
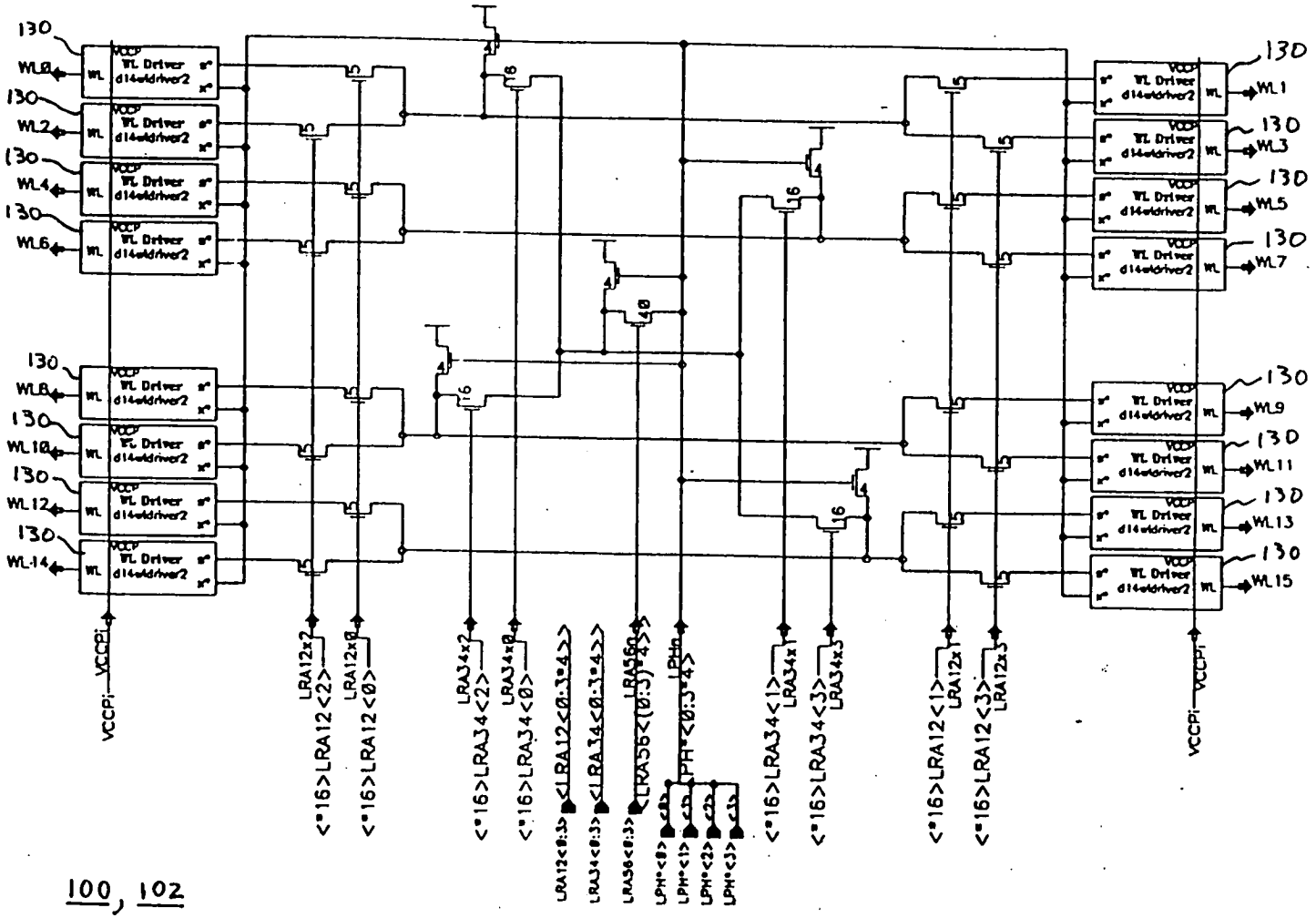

28
110
RAEN*
RA*<0>
RA<0>
Row 2to1 Predecode
d14predec_row2to1
EVEN
ODD
Row Addr 4to1 Predecode
d14predec_row4to1
112
RA*<1>
RA<1>
RA*<2>
RA<2>
RA12<0:3>
RA*<3>
RA<3>
RA*<4>
RA<4>
114
RA34<0:3>
RA*<5>
RA<5>
RA*<6>
RA<6>
116
RA56<0:3>
RA*<7>
RA<7>
RA*<8>
RA<8>
118
RA78<0:3>
RA*<9>
RA<9>
RA*<10>
RA<10>
120
RA910<0:3>
122
RA*<11>
RA<11>
RA_11<0:1>
RA*<12>
RA<12>
RA_12<0:1>
124

FIGURE 19



100, 102

FIGURE 20

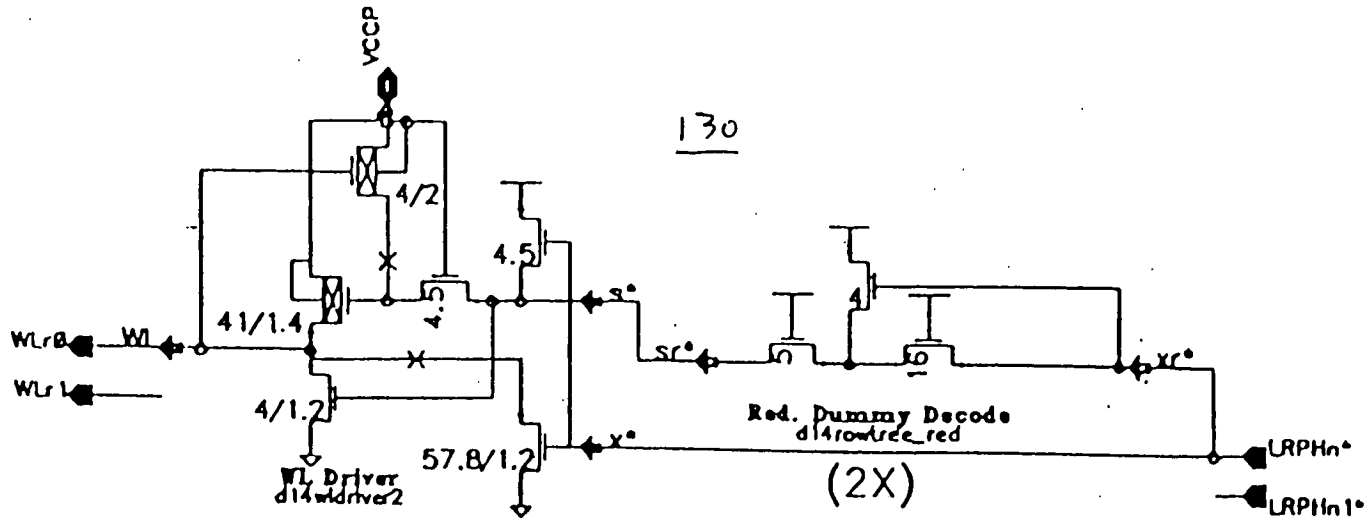

VCCP
130
4/2
4.5
41/1.4
4/1.2
57.8/1.2
WLrB
WL
WLr1
WL Driver
d14wldriver2
Red. Dummy Decode
d14rowdec_red
(2X)
LRPHn*
LRPHn1*

FIGURE 21

Laser/Electrical Fuse Options

OPT4KREF

not blown	8K Refresh (default)
blown	4K Refresh

OPTFAST

not blown	slow (default)
blown	fast

OPTS

not blown	fast-page (default)
blown	static column

ROWRED

not blown	not used
blown	not used

COLRED

not blown	fast EQIO/EQSA (default)
blown	slow EQIO/EQSA

OPTSRB	OPTSRA	Ref Rate
not blown	not blown	128ms (Default)
not blown	blown	192ms
blown	not blown	256ms
blown	blown	64ms

ENTOPO

not blown	data topo on (default)
blown	data topo off

Bonding Options

XOPTA	XOPTB	
NO	NO	OPTX16 (default)
NO	VCC	OPTX8
VCC	NO	OPTX4
VCC	VCC	OPTX1

OPTEDO

NO	no EDO (default)
VSS	EDO

Option Fuse	Option Fuse Selection Address					
	A10	A9	A8	A7	A6	A5
OPT4KREF	1	1	1	0	0	0
OPTS	1	1	1	0	0	1
OPTFAST	1	1	1	0	1	0
ROWRED	1	1	1	0	1	1
COLRED	1	1	1	1	0	0
OPTSRA	1	1	1	1	0	1
OPTSRB	1	1	1	1	1	0
ENTOPO	1	1	1	1	1	1

FIGURE 22

INPUTS OUTPUTS

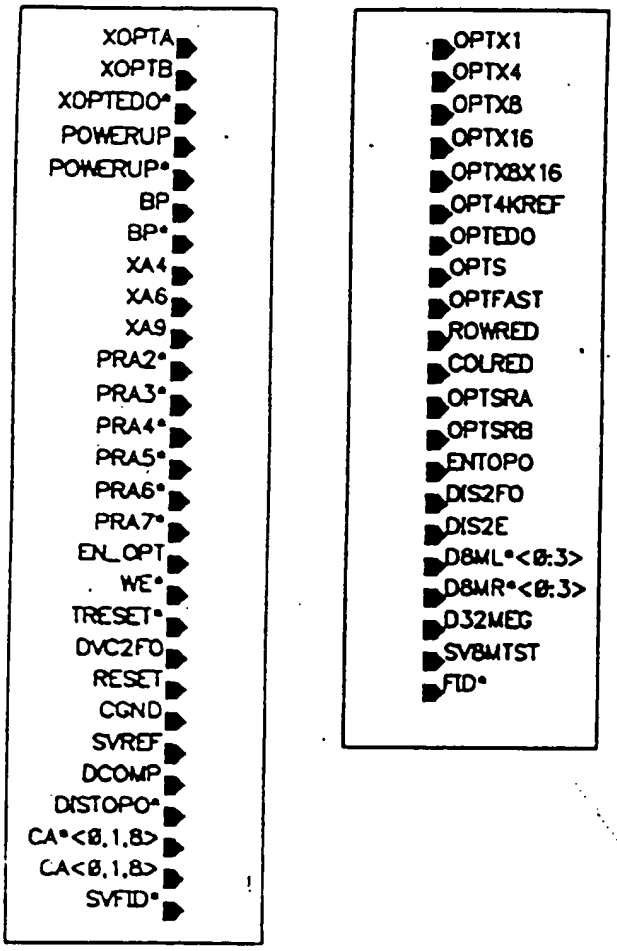


FIGURE 23

32MEG OPTION LOGIC

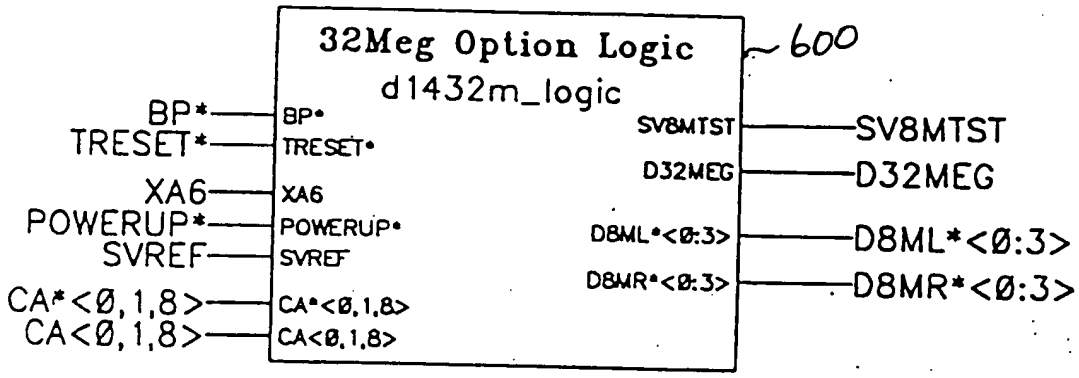


FIGURE 24

BONDING OPTIONS

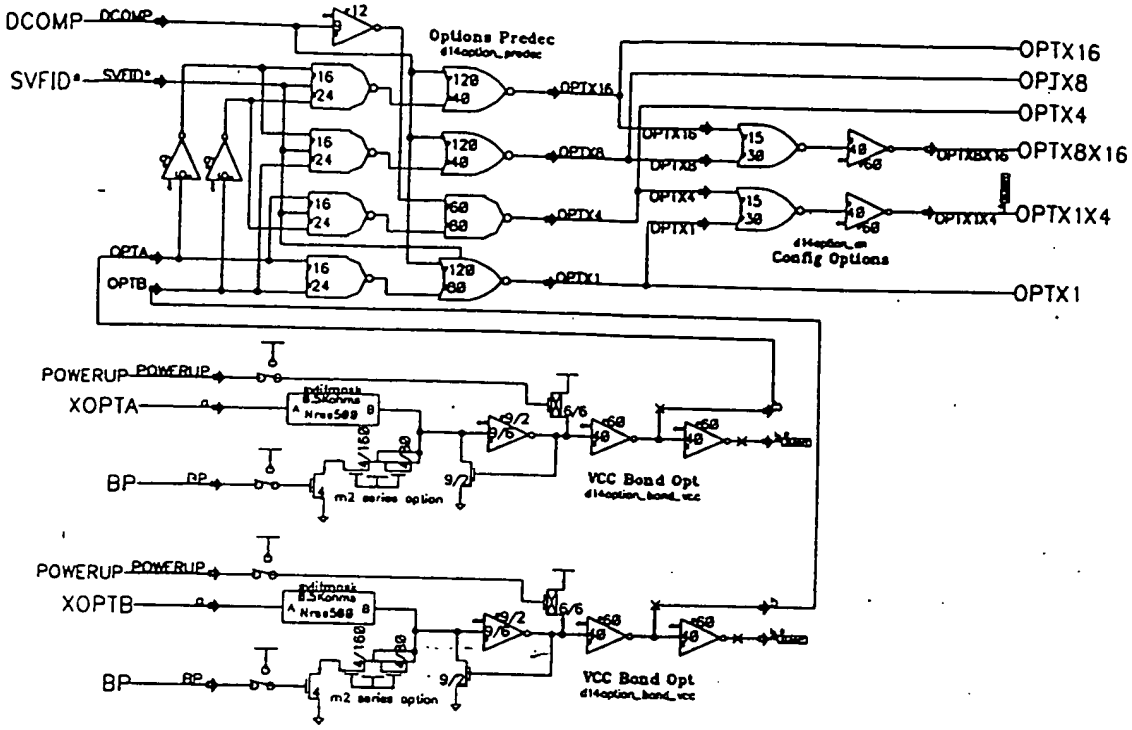


FIGURE 25

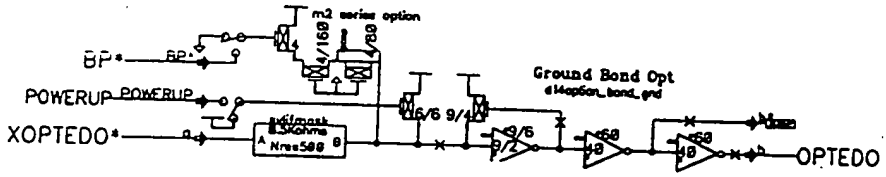


FIGURE 26

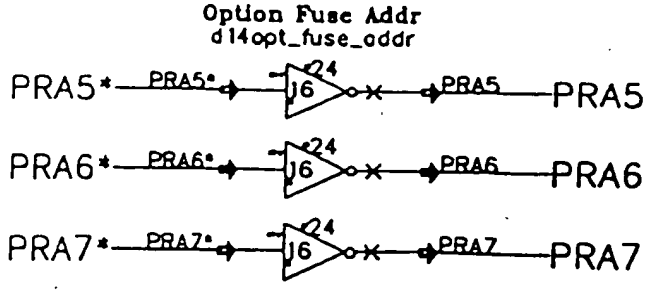


FIGURE 27

LASER FUSE I.D. ADDRESS

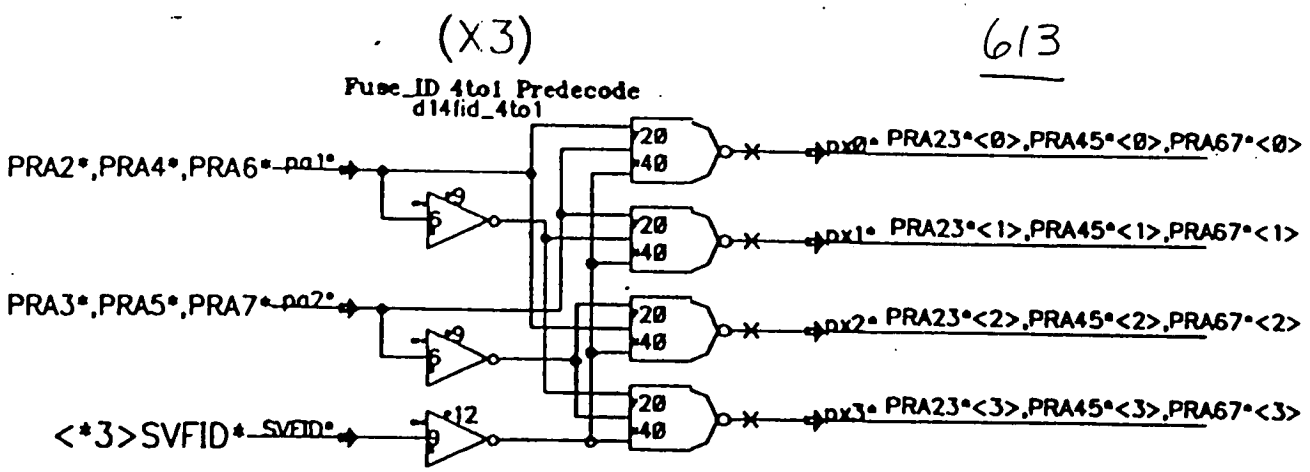


FIGURE 28

LASER FUSE I.D.

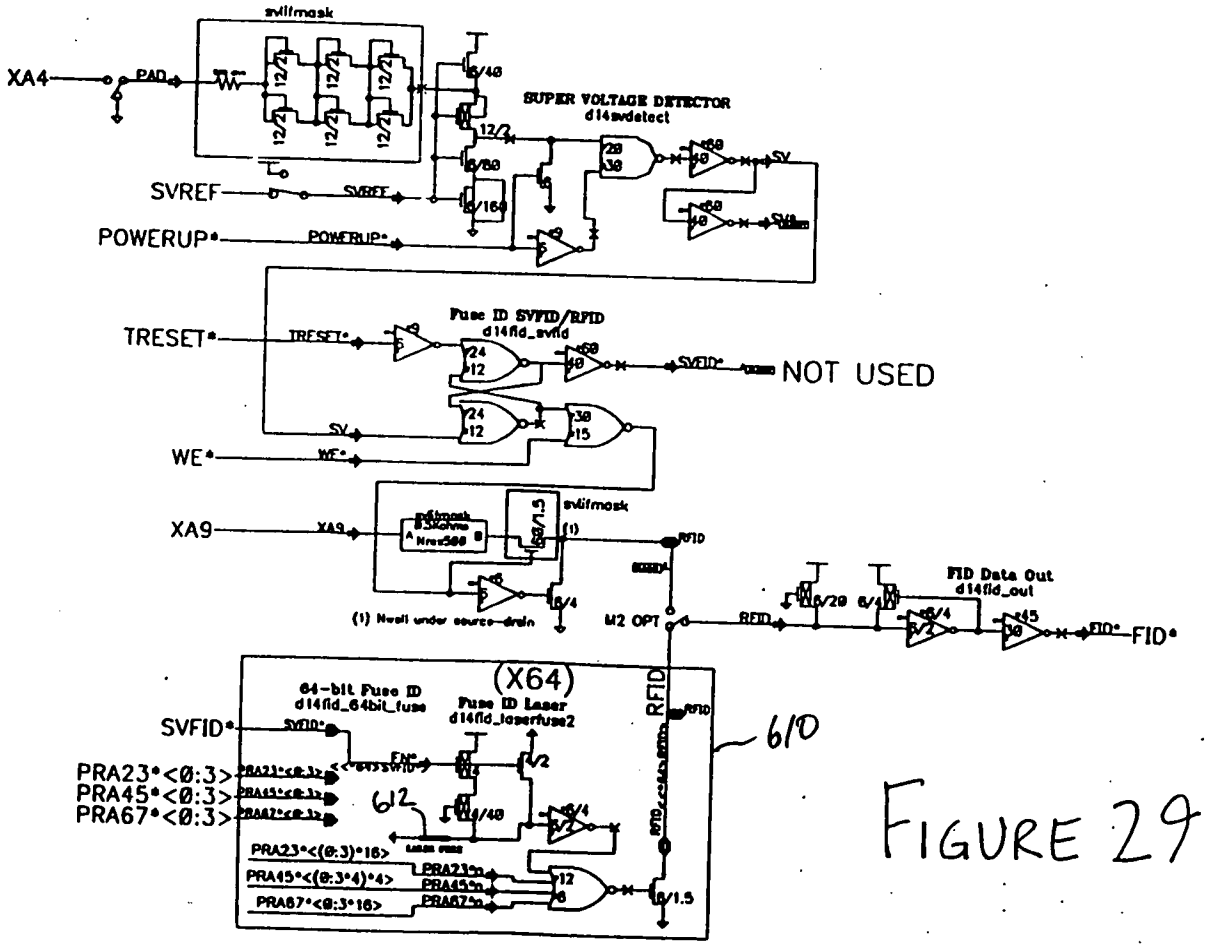


FIGURE 29

Fuse Blown = Logic "1"

LASER/ELECT FUSE OPTIONS

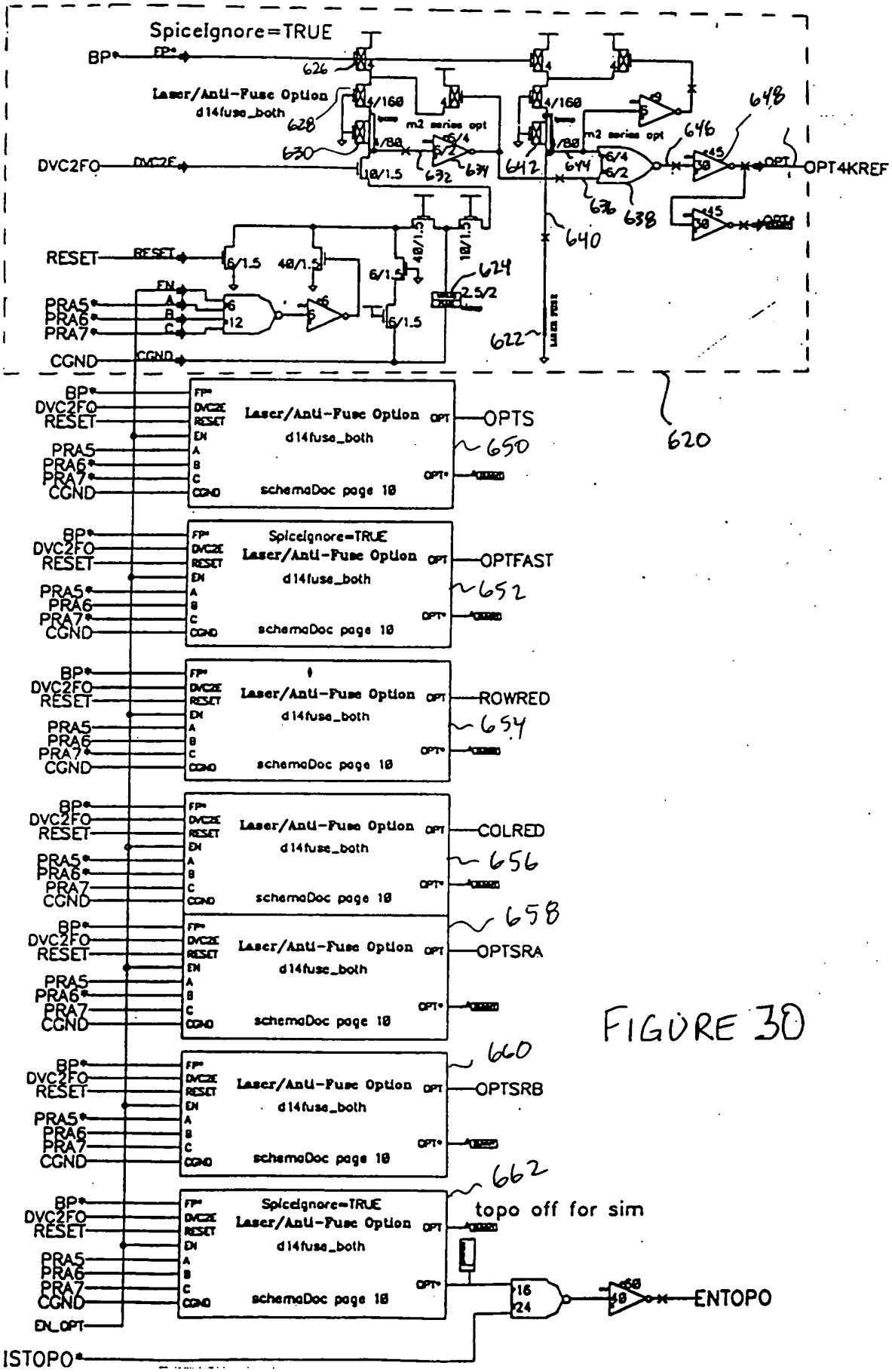
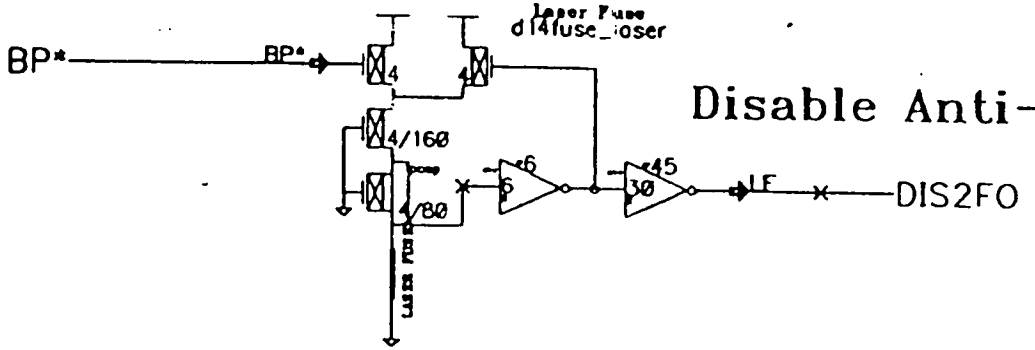
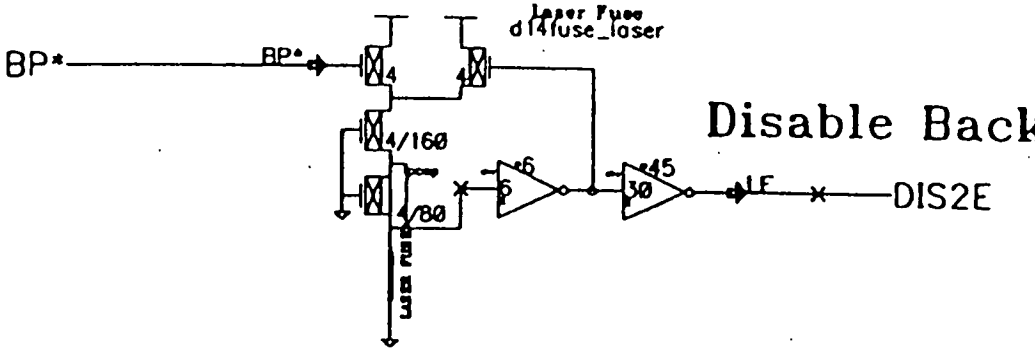


FIGURE 30



Disable Anti-fuse Option

FIGURE 31



Disable Backend Repair

FIGURE 32

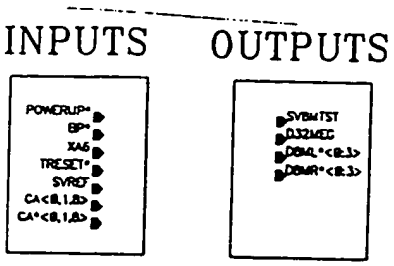


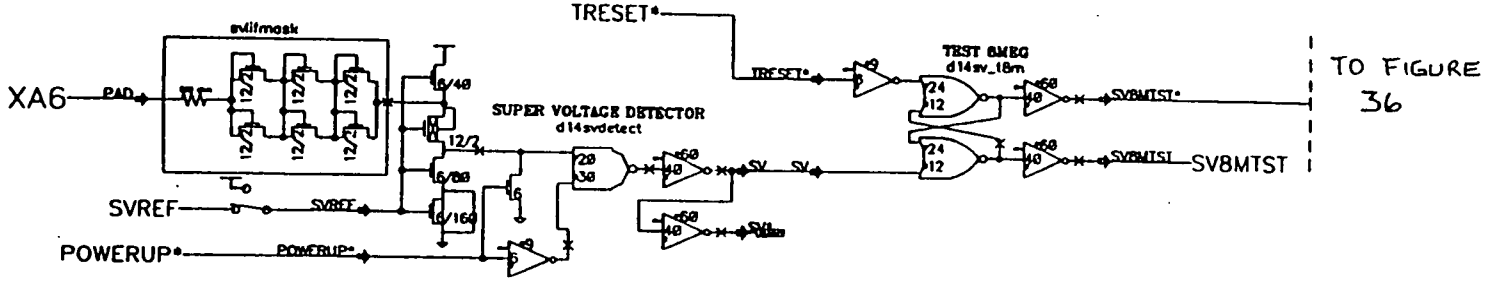
FIGURE 34

8Meg Array ICC–standby test

A1	A8	A7	Signal De–activated	Array Section Enabled (Ref to X4)
Ø	Ø	Ø	D8ML*<Ø>	LEFT DQØ
Ø	Ø	1	D8MR*<Ø>	RIGHT DQØ
Ø	1	Ø	D8ML*<1>	LEFT DQ1
Ø	1	1	D8MR*<1>	RIGHT DQ1
1	Ø	Ø	D8ML*<2>	LEFT DQ2
1	Ø	1	D8MR*<2>	RIGHT DQ2
1	1	Ø	D8ML*<3>	LEFT DQ3
1	1	1	D8MR*<3>	RIGHT DQ3

FIGURE 33

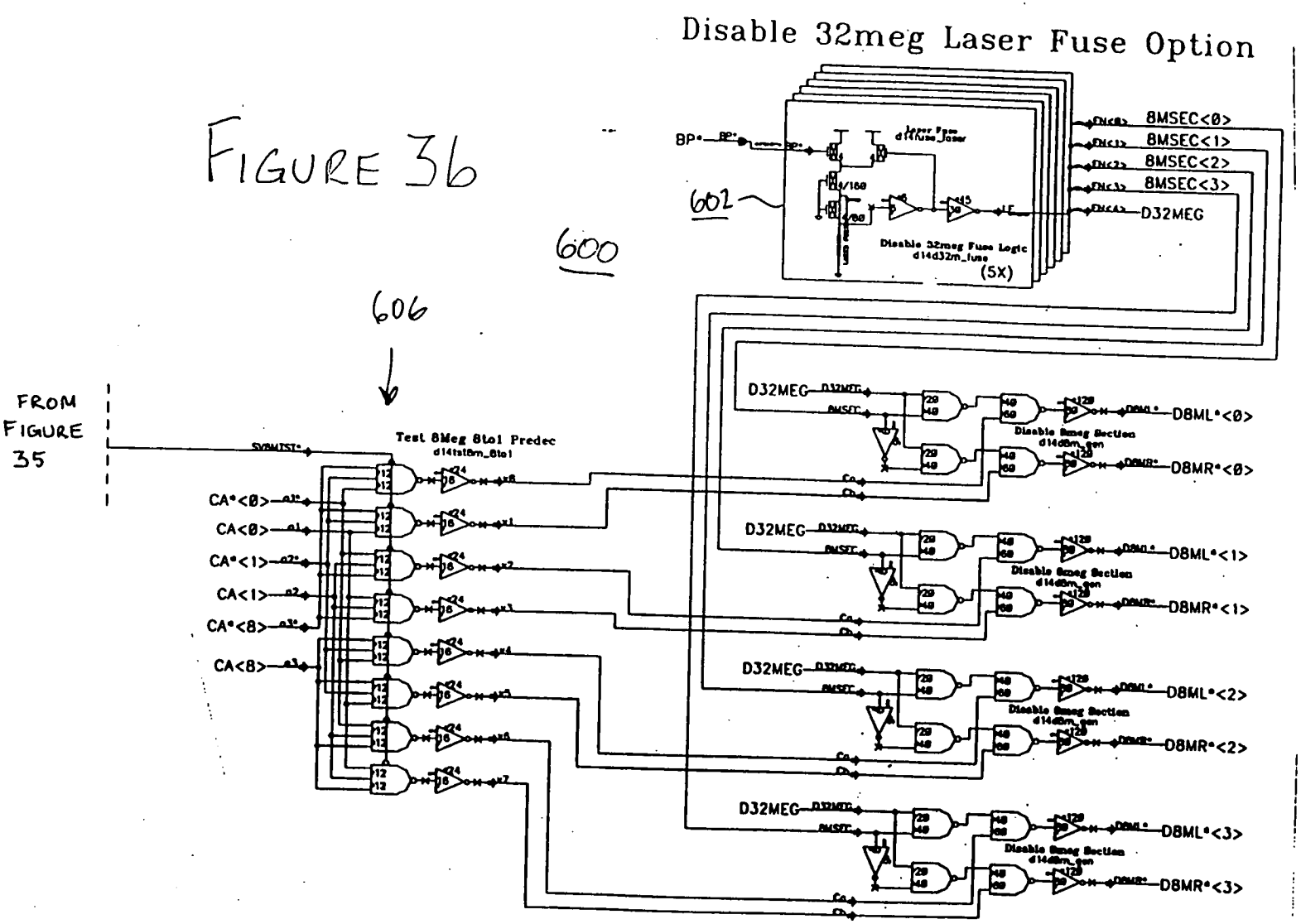
XA6 Supervoltage Detect/Latch 600



604

FIGURE 35

FIGURE 36


Disable 32meg Laser Fuse Option
600
602
606
BP*
8MSEC<0>
8MSEC<1>
8MSEC<2>
8MSEC<3>
D32MEG
Disable 32meg Fuse Logic
d14d32m_fuse
(5X)
FROM FIGURE 35
Test 8Meg 8to1 Predec
d14ts18m_8to1
CA*<0>
CA<0>
CA*<1>
CA<1>
CA*<8>
CA<8>
D8ML*<0>
D8MR*<0>
D8ML*<1>
D8MR*<1>
D8ML*<2>
D8MR*<2>
D8ML*<3>
D8MR*<3>
Disable 8meg Section
d14d8m_gen

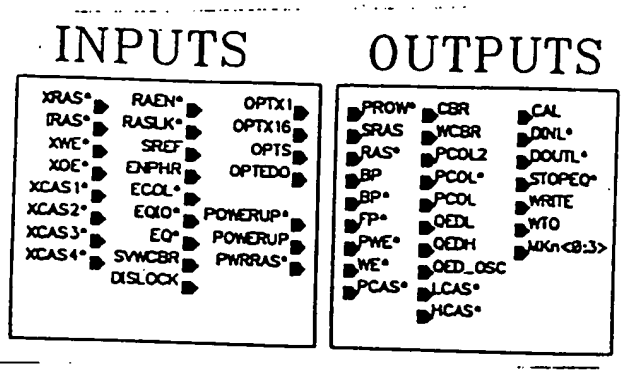


FIGURE 37

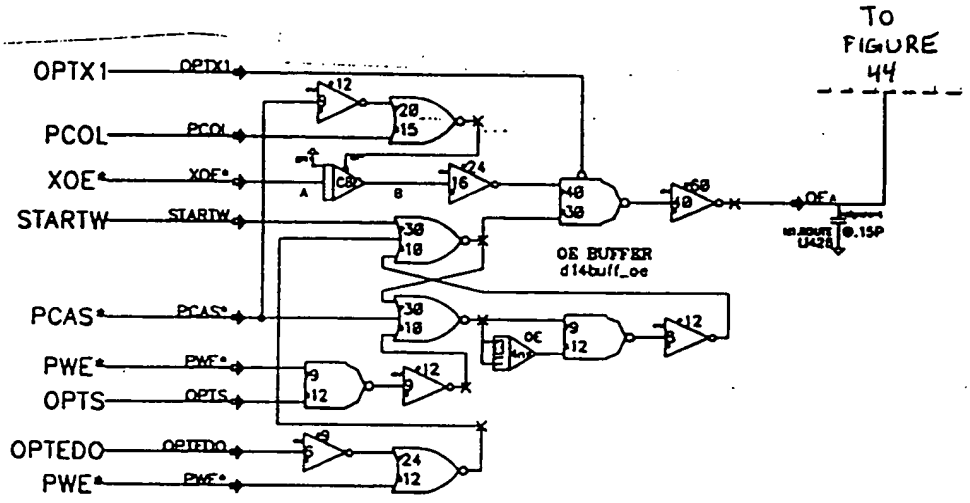


FIGURE 38

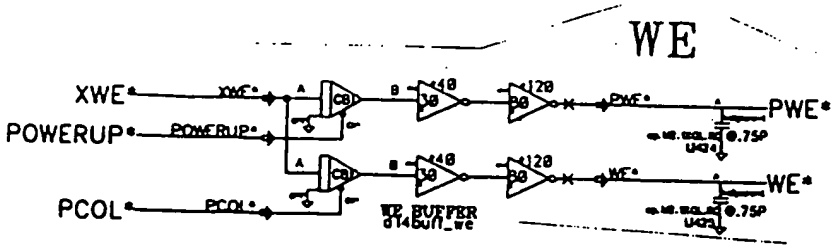


FIGURE 39

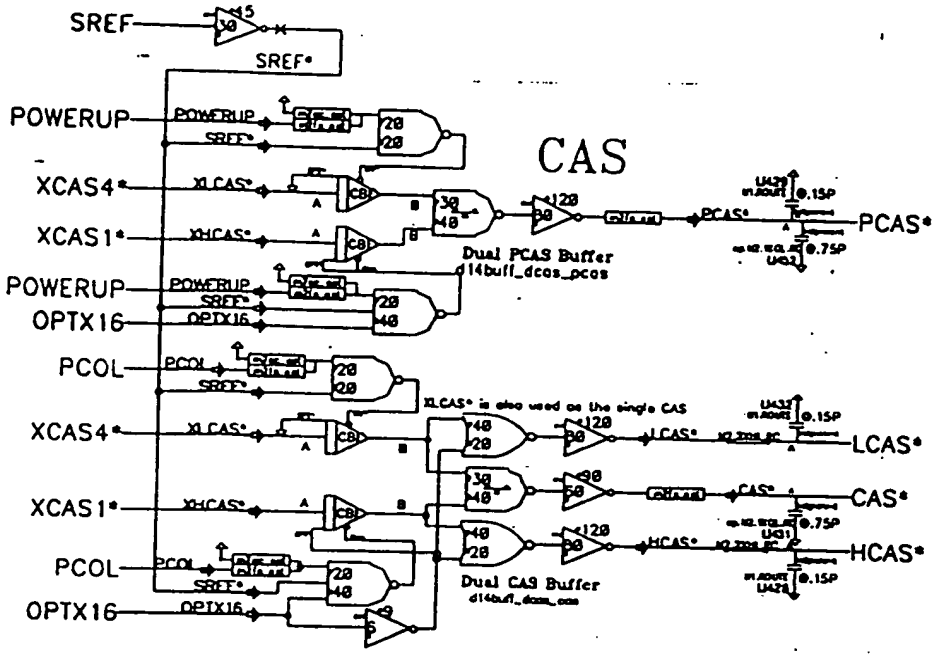


FIGURE 40

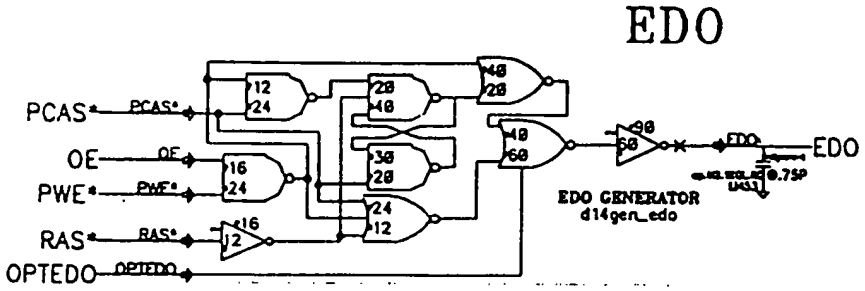


FIGURE 41

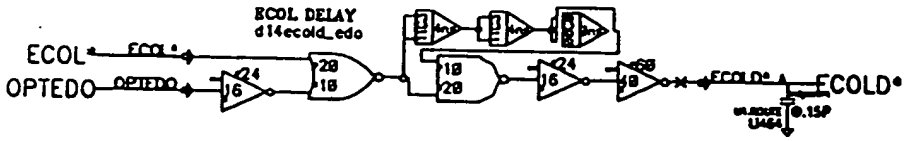


FIGURE 42

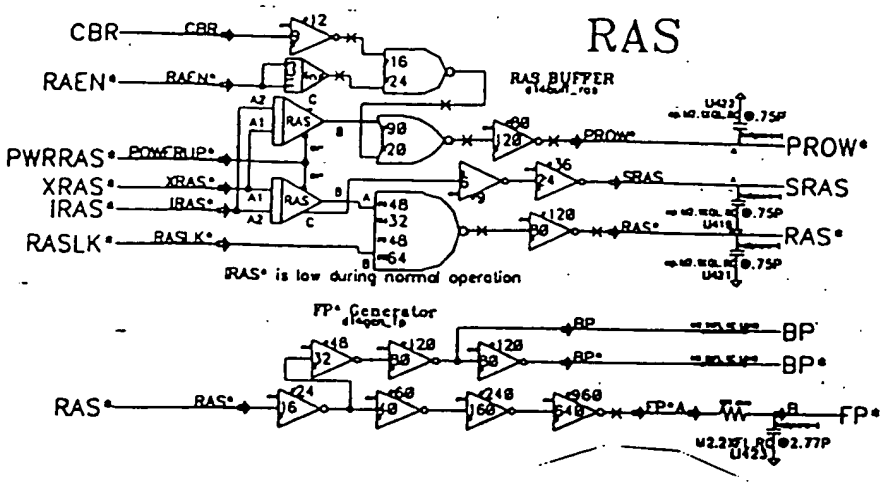

RAS
CBR
RAEN*
PWRRAS*
XRAS*
IRAS*
RASLK*
RAS BUFFER
PROW*
SRAS
RAS*
IRAS* is low during normal operation
FP* Generator
BP
BP*
FP*

FIGURE 43

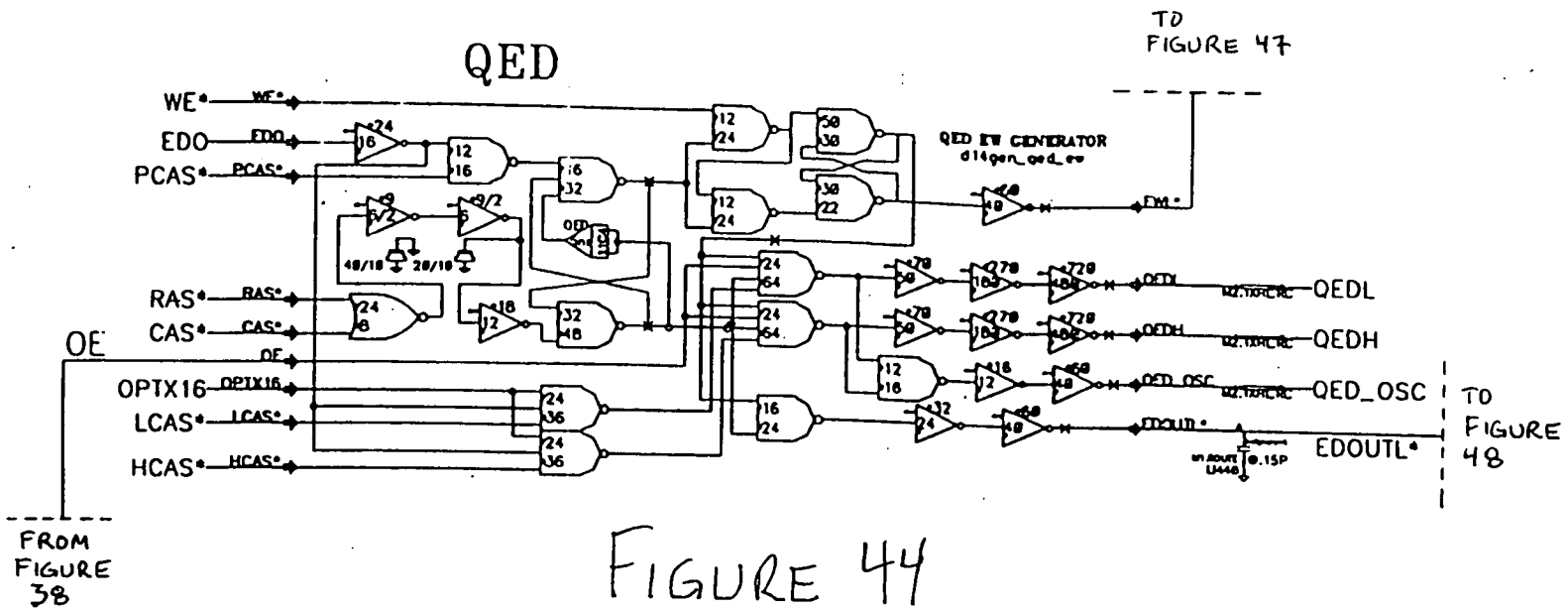

QED
TO FIGURE 47
WE*
EDO
PCAS*
RAS*
CAS*
OE
OPTX16
LCAS*
HCAS*
QED EW GENERATOR
QEDL
QEDH
QED_OSC
EDOUTL*
TO FIGURE 48
FROM FIGURE 38

FIGURE 44

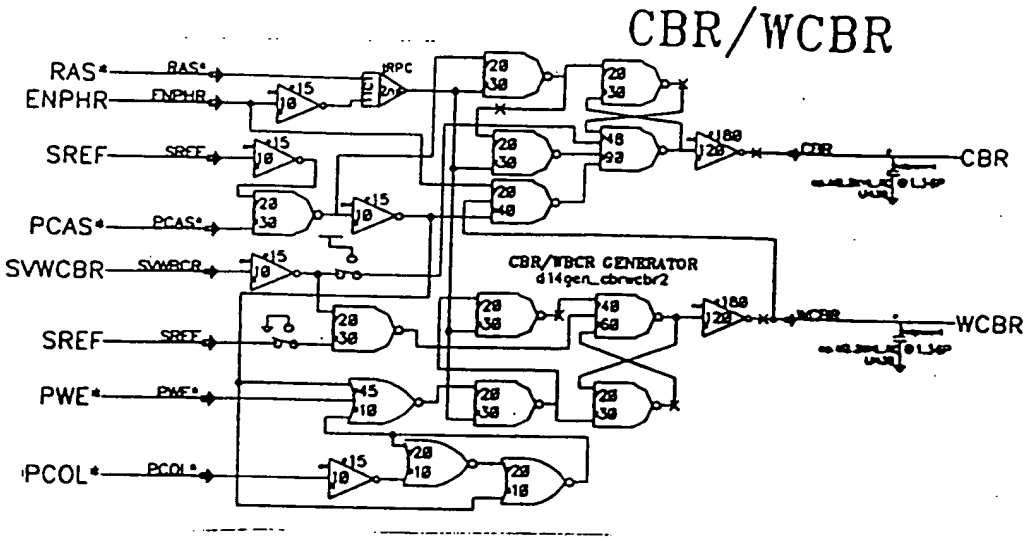

CBR/WCBR
RAS*
ENPHR
SREF
PCAS*
SVWCBR
SREF
PWE*
PCOL*
CBR/WBCR GENERATOR
d14gen_cbrwcbr2
CBR
WCBR

FIGURE 45

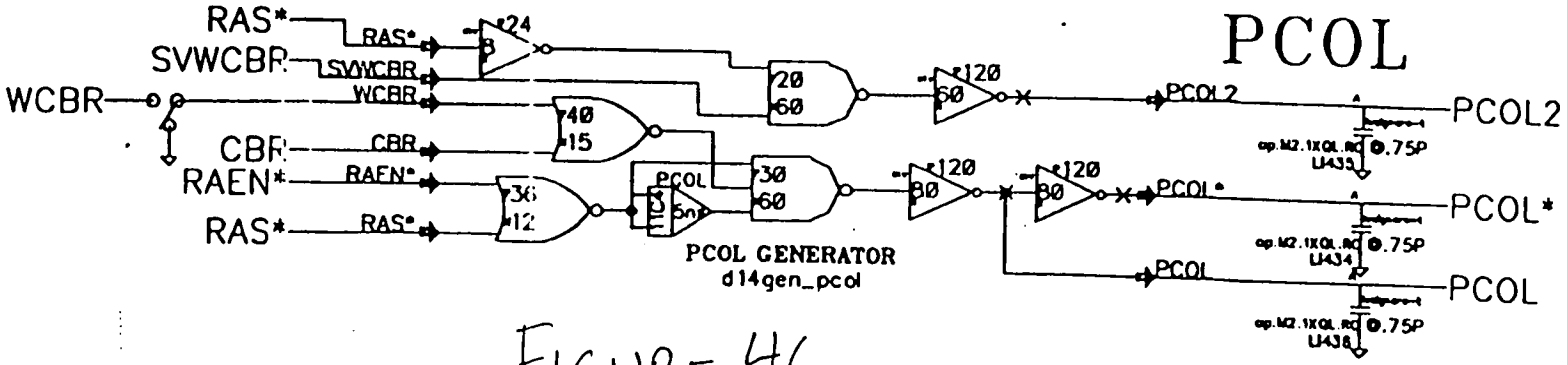


FIGURE 46

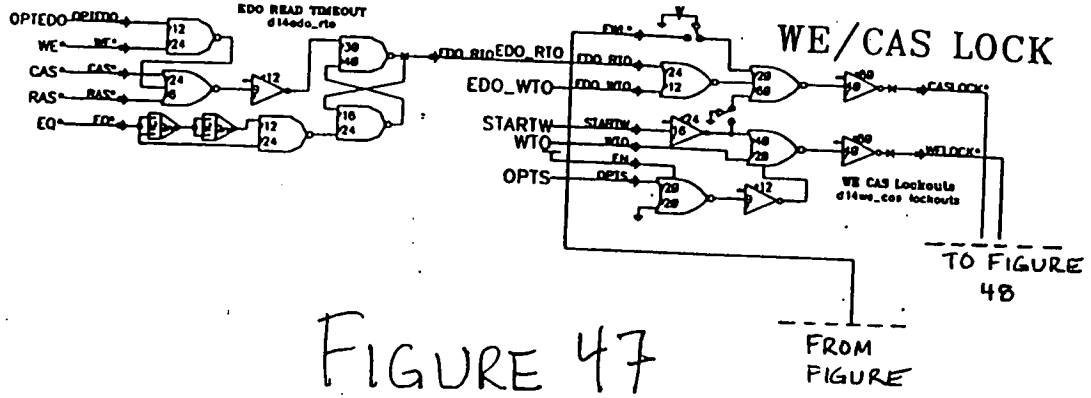


FIGURE 47

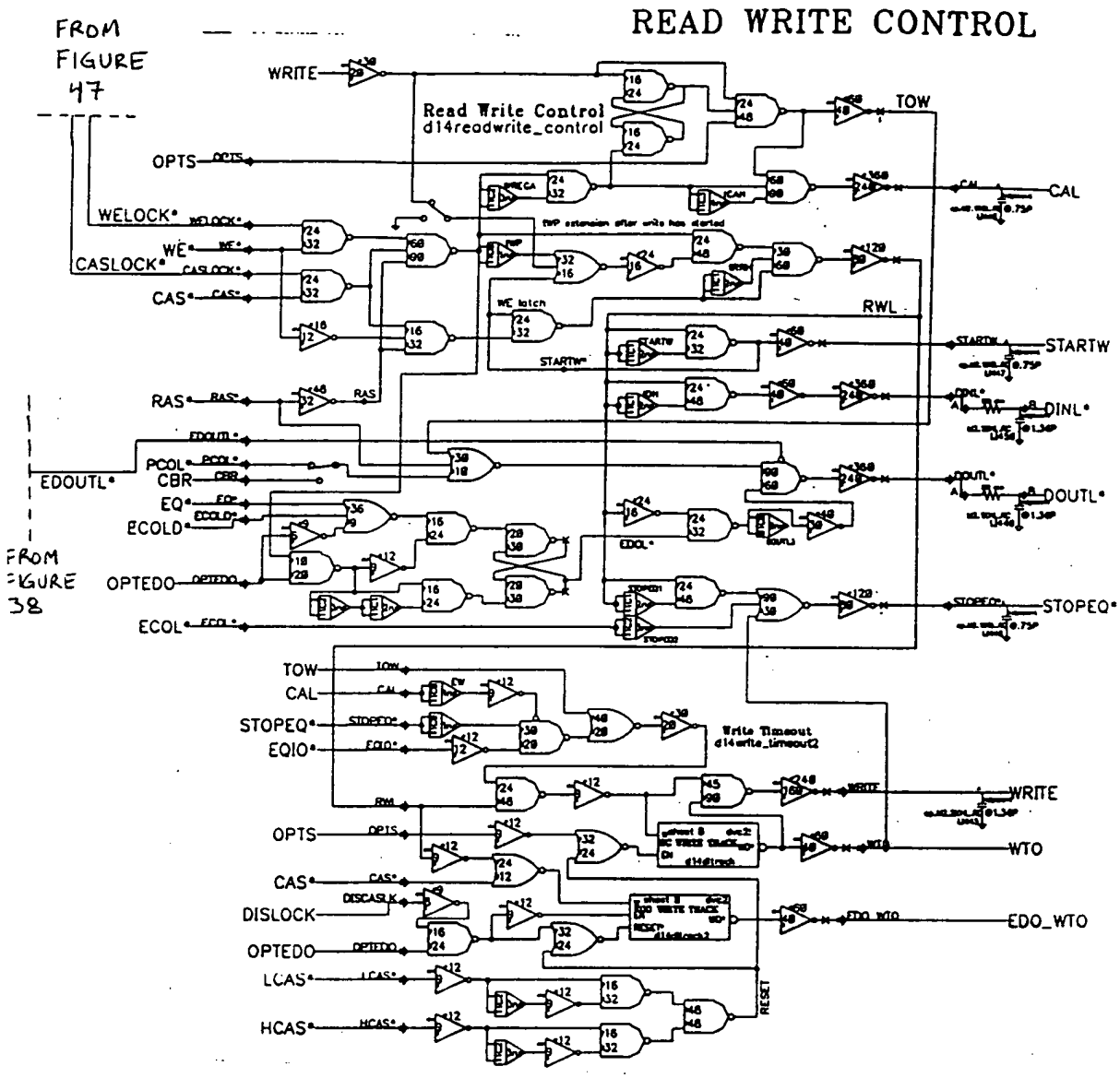

READ WRITE CONTROL
FROM FIGURE 47
FROM FIGURE 38
Read Write Control
d14readwrite_control
WRITE
OPTS
WELOCK*
WE*
CASLOCK*
CAS*
RAS*
EDOUTL*
PCOL*
CBR*
EQ*
ECOLD*
OPTEDO*
ECOL*
TOW
CAL
STOPEQ*
EQIO*
RWL
STARTW
DINL*
DOUTL*
STOPEQ*
WRITE
WTO
EDO_WTO
DISCASLK
DISLOCK
LCAS*
HCAS*
RESET
Write Timeout
d14write_timeout2

FIGURE 48

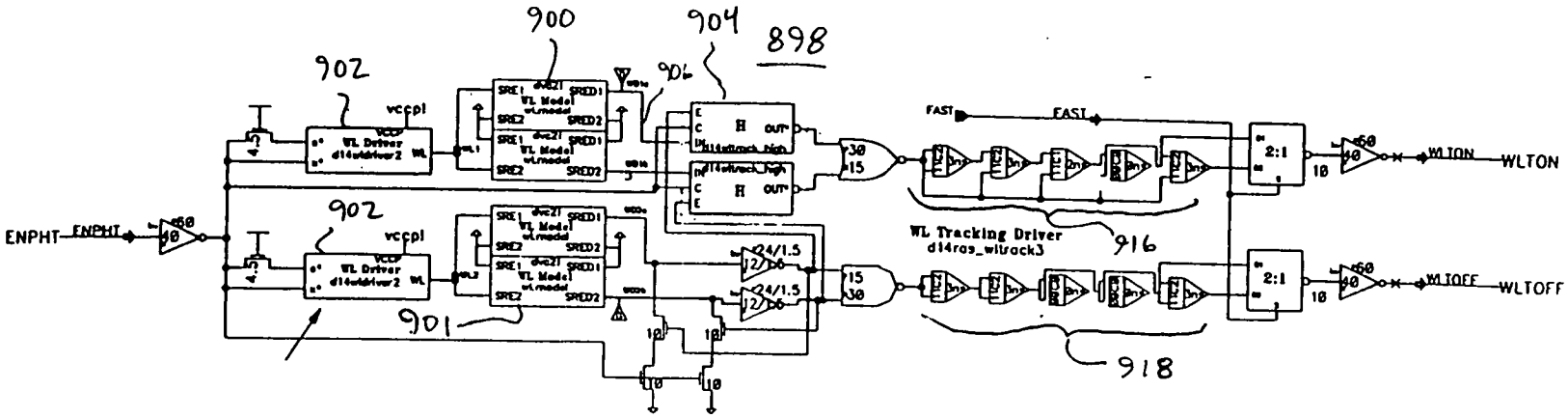


FIGURE 49

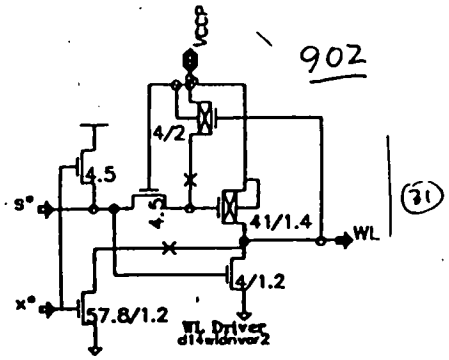


FIGURE 50

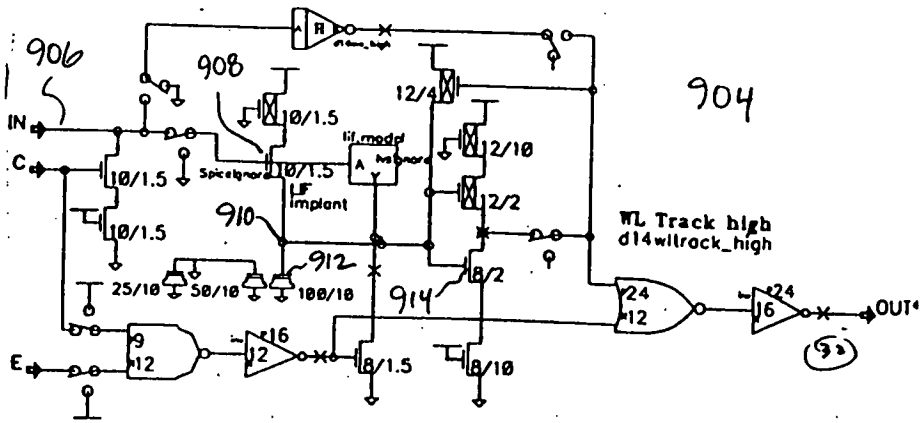


FIGURE 51

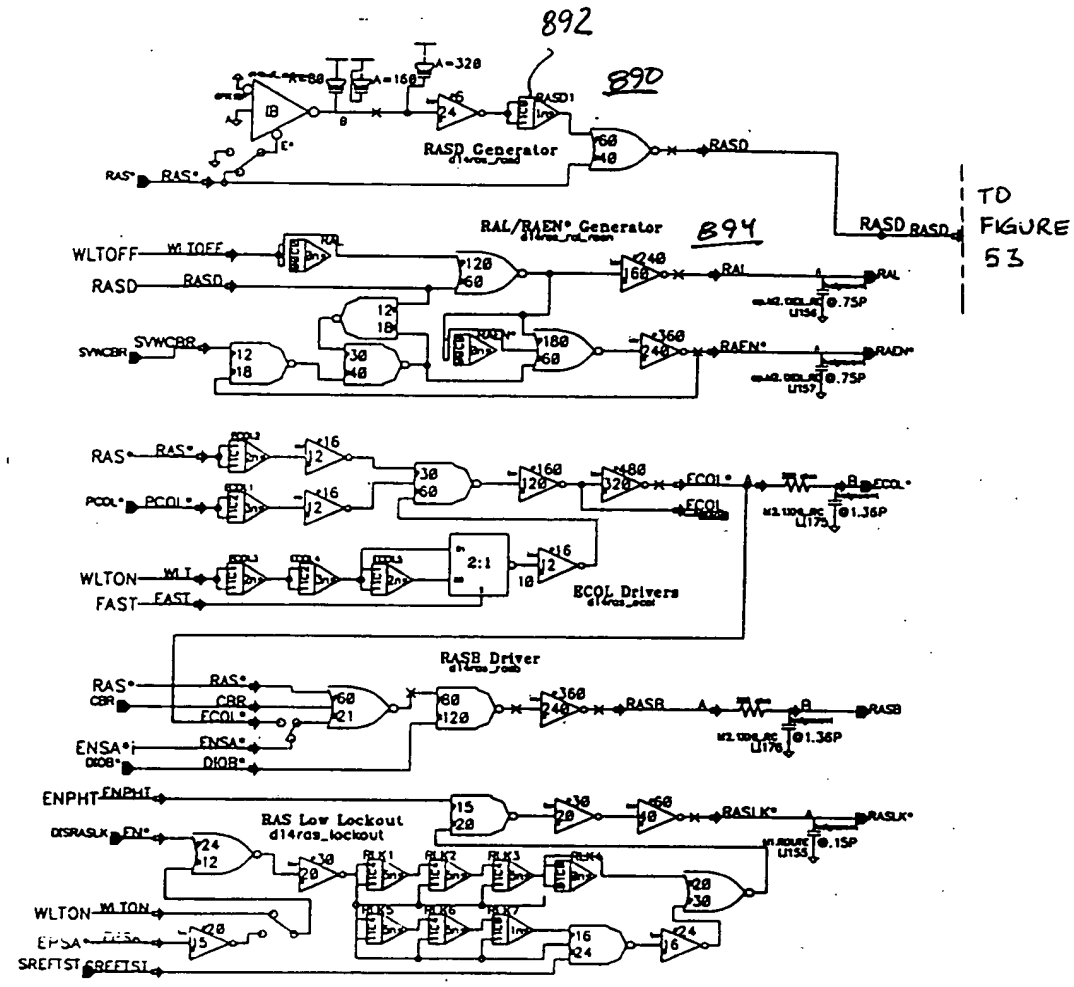

892
890
RASD Generator
RASD
RAS
RAS*
TO FIGURE 53
RAL/RAEN* Generator
894
WLTOFF
RASD
SVWCBR
RAL
RAEN*
ECOL Drivers
WLTON
FAST
2:1
RASB Driver
CBR
ENSA*
ENPHT
RAS Low Lockout
d14rds_lockout
WLTON
SREFTST

FIGURE 52

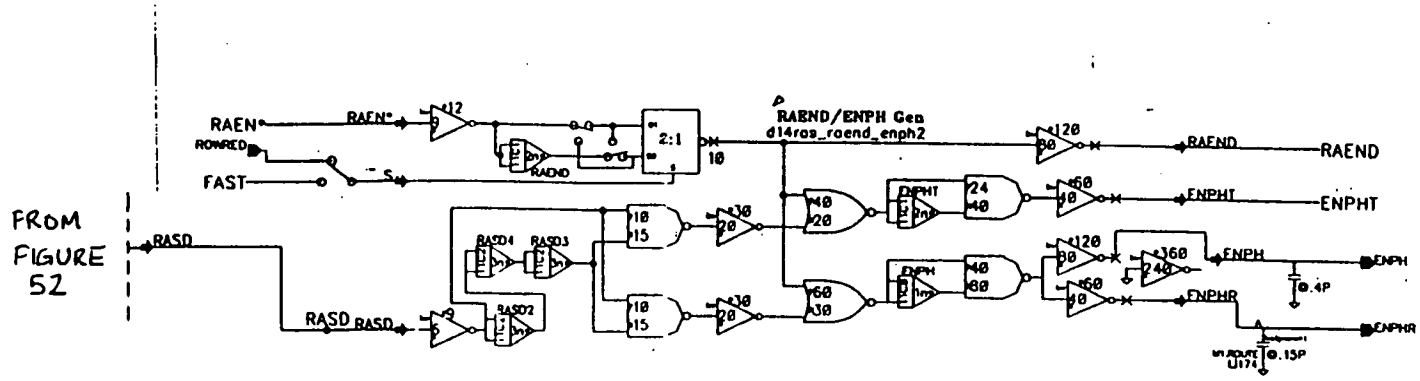


FIGURE 53

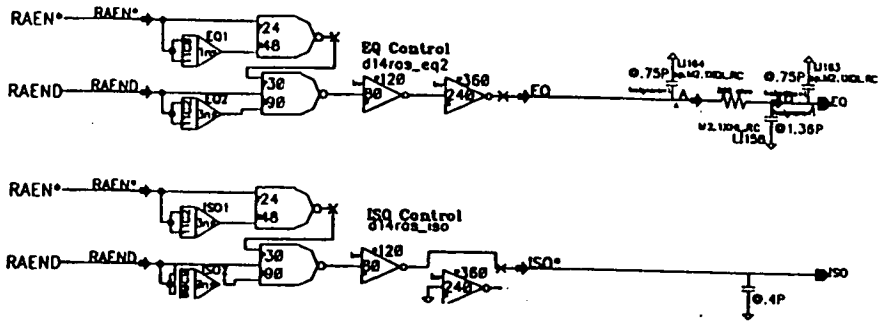


FIGURE 54

920

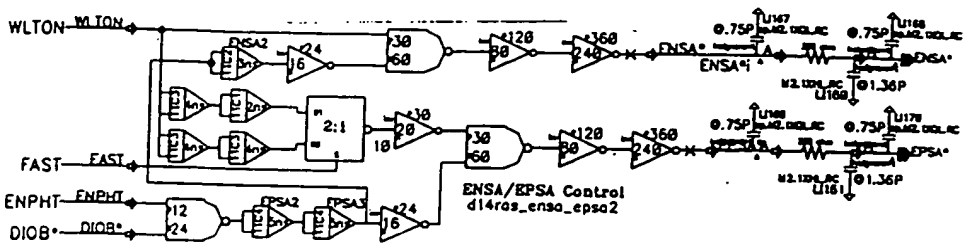


FIGURE 55

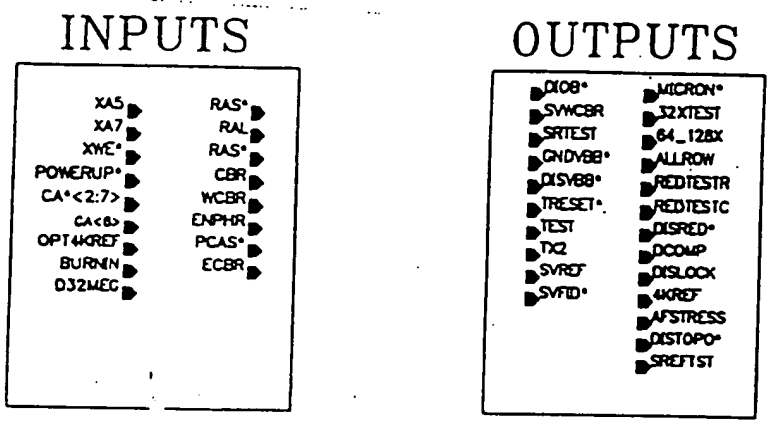

INPUTS
XA5
XA7
XWE*
POWERUP*
CA*<2:7>
CA<8>
OPT4KREF
BURNIN
D32MEG
RAS*
RAL
RAS*
CBR
WCBR
ENPHR
PCAS*
ECBR
OUTPUTS
DIOB*
SVWCBR
SRTEST
GNDVBB*
DISVBB*
TRESET*
TEST
TX2
SVREF
SVFID*
MICRON*
32XTEST
64_128X
ALLROW
REDTESTR
REDTESTC
DISRED*
DCOMP
DISLOCK
4KREF
AFSTRESS
DISTOPO*
SREFTST

FIGURE 56

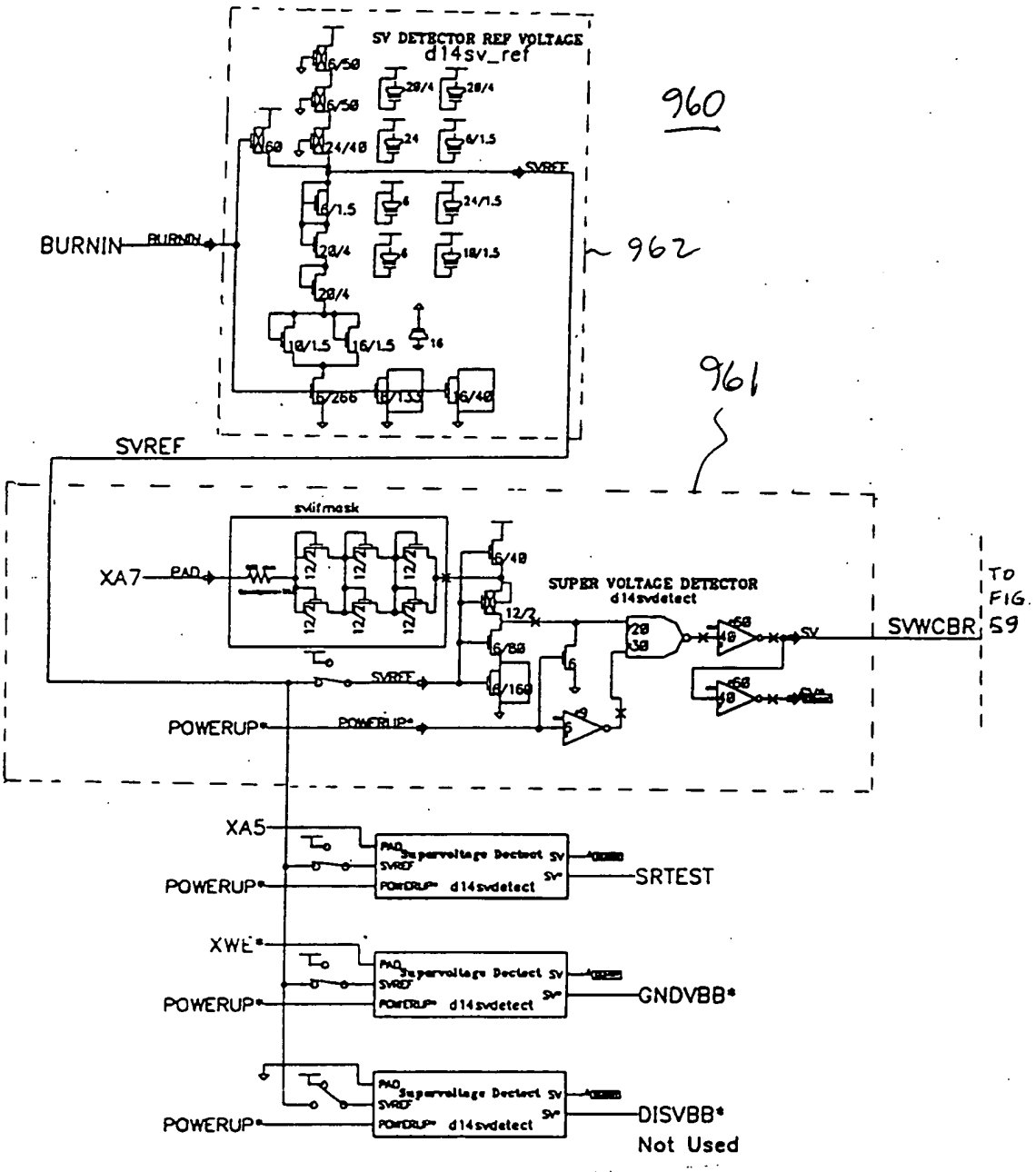


FIGURE 57

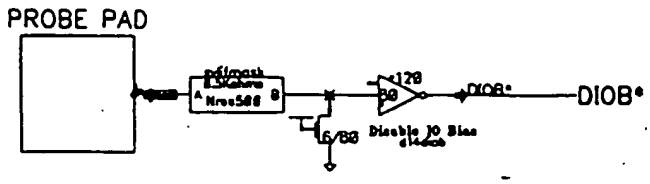


FIGURE 58

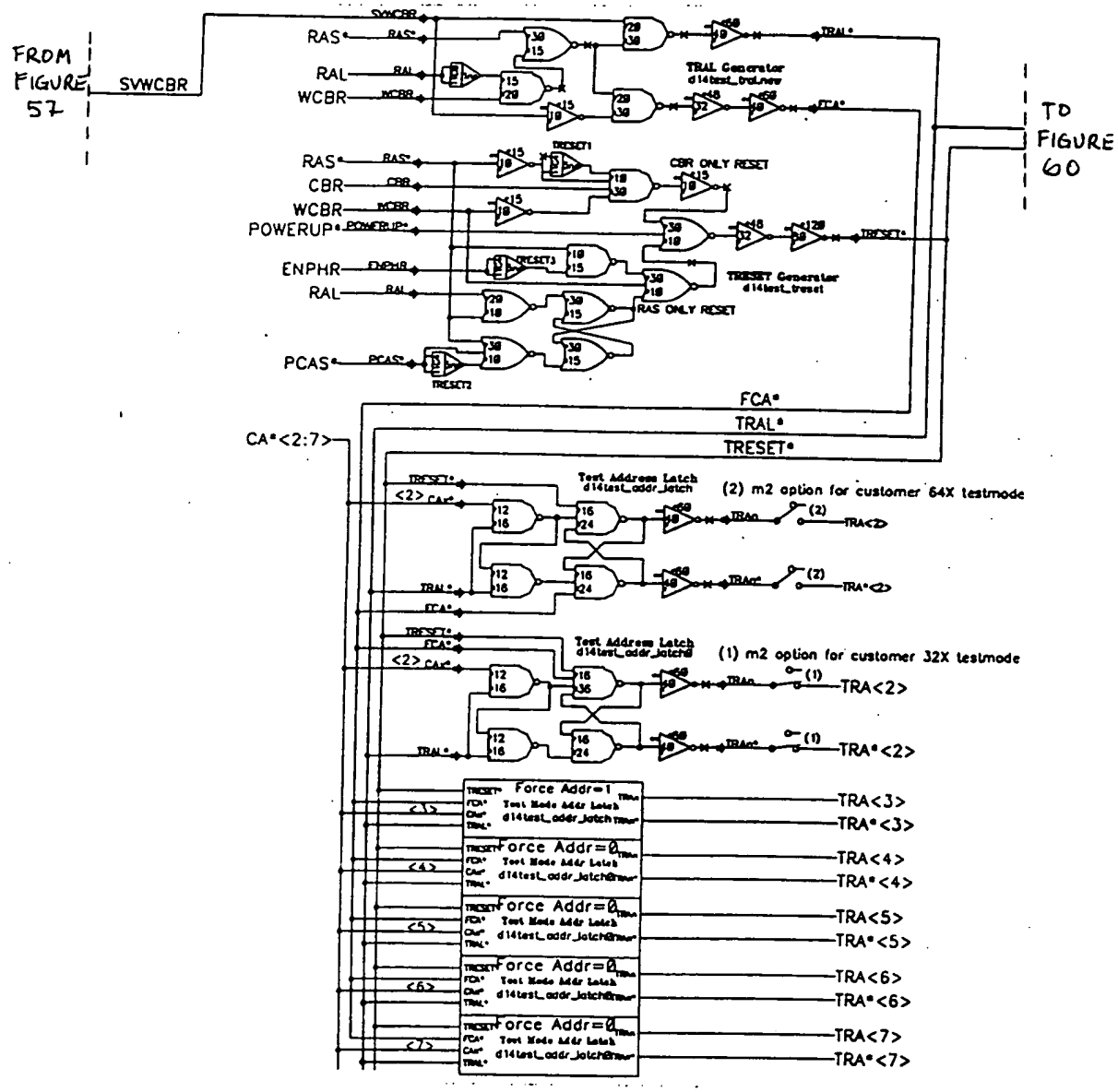

FROM FIGURE 57
SVWCBR
RAS
RAL
WCBR
TRAL Generator
d14test_tral.new
TO FIGURE 60
CBR
POWERUP
ENPHR
PCAS
CBR ONLY RESET
RAS ONLY RESET
TRESET Generator
d14test_treset
FCA
TRAL
TRESET
CA<2:7>
Test Address Latch
d14test_addr_latch
(2) m2 option for customer 64X testmode
(1) m2 option for customer 32X testmode
Force Addr=1
Force Addr=0
TRA<2>
TRA*<2>
TRA<3>
TRA*<3>
TRA<4>
TRA*<4>
TRA<5>
TRA*<5>
TRA<6>
TRA*<6>
TRA<7>
TRA*<7>

FIGURE 59

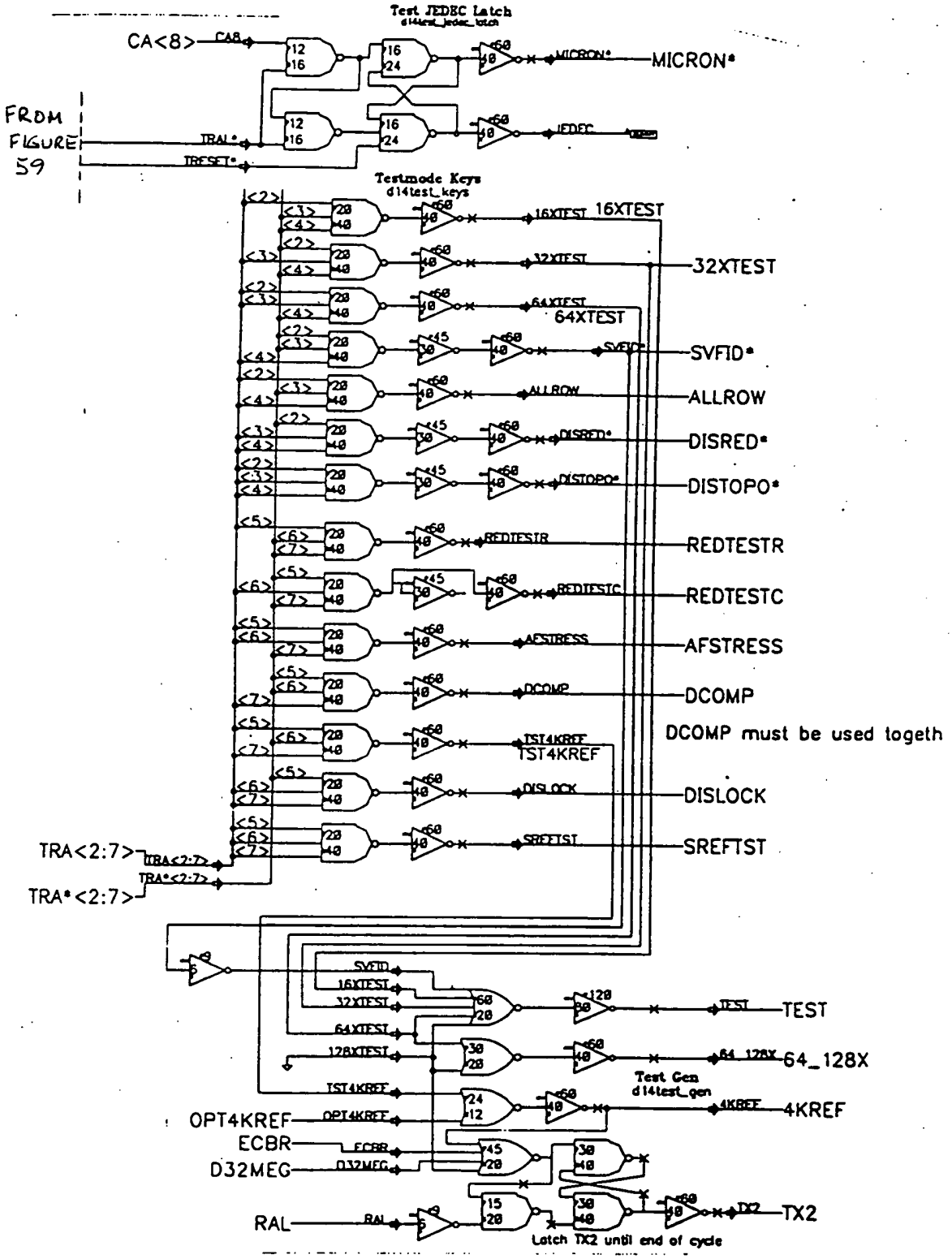

Test JEDEC Latch
CA<8>
MICRON*
MICRON
FROM FIGURE 59
TRA*
TRESET*
JEDEC
Testmode Keys
d14test_keys
16XTEST
16XTEST
32XTEST
32XTEST
64XTEST
64XTEST
SVFID*
SVFID
ALLROW
ALLROW
DISRED*
DISRED*
DISTOPO*
DISTOPO*
REDTESTR
REDTESTR
REDTESTC
REDTESTC
AFSTRESS
AFSTRESS
DCOMP
DCOMP
DCOMP must be used togeth
TST4KREF
TST4KREF
DISLOCK
DISLOCK
SREFTST
SREFTST
TRA<2:7>
TRA*<2:7>
TEST
TEST
64_128X
64_128X
Test Gen
d14test_gen
4KREF
4KREF
OPT4KREF
ECBR
D32MEG
RAL
TX2
TX2
Latch TX2 until end of cycle

FIGURE 60

Test Mode Address Keys

A1	A0	A6	A5	A4	A3	A2	TEST MODE
–	–	–	–	0	0	0	no test
–	–	–	–	0	0	1	16X test
–	–	–	–	0	1	0	32X test
–	–	–	–	0	1	1	64X test
–	–	–	–	1	0	0	Fuse I.D.
–	–	–	–	1	0	1	Disable DVC2 w/ all rows high
–	–	–	–	1	1	0	Disable redundant element
–	–	–	–	1	1	1	Disable Data Topo
–	0	0	0	–	–	–	no test
–	0	0	1	–	–	–	Row redundant element pretest
–	0	1	0	–	–	–	Column redundant element pretest
–	0	1	1	–	–	–	Anti-fuse Stress test
–	1	0	0	–	–	–	Test Data compression
–	1	0	1	–	–	–	4K refresh (otherwise 8K ref)
–	1	1	0	–	–	–	Disable RAS/CAS lockout
–	1	1	1	–	–	–	Self-refresh Test
0	–	–	–	–	–	–	JEDEC test mode
1	–	–	–	–	–	–	MICRON test mode

FIGURE 61

Supervoltage and Backend Programing Inputs

Input Pad	Description of Usage	Page
A0	generates PRGCANR } only if SVPRG is high	8
A1	generates PRGCANC } only if SVPRG is high	8
A2	generates PRGR } only if SVPRG is high	8
A3	generates PRGC } only if SVPRG is high	8
A4	supervoltage – Not Used	4a
A5	supervoltage – self refresh test	7
A6	supervoltage – 8Meg ICC test	4b
A7	supervoltage – WCBR	7
A10	anti-fuse programming voltage	8
A11	supervoltage – elect fuse program SVPRG	8
WE	supervoltage – ground VBB	7

FIGURE 62

JEDEC/MICRON Testmode

READ DATA	OUTPUT	
	JEDEC	MICRON
All 0's	1	0
All 1's	1	1
Different	0	Tristate

FIGURE 63

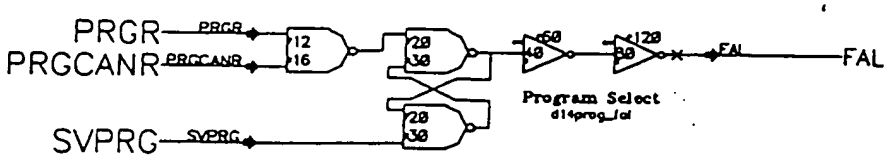


FIGURE 65

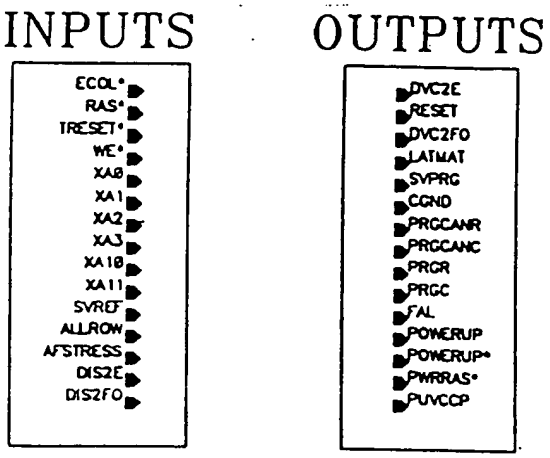


FIGURE 64

BACKEND REPAIR PROGRAMMING LOGIC

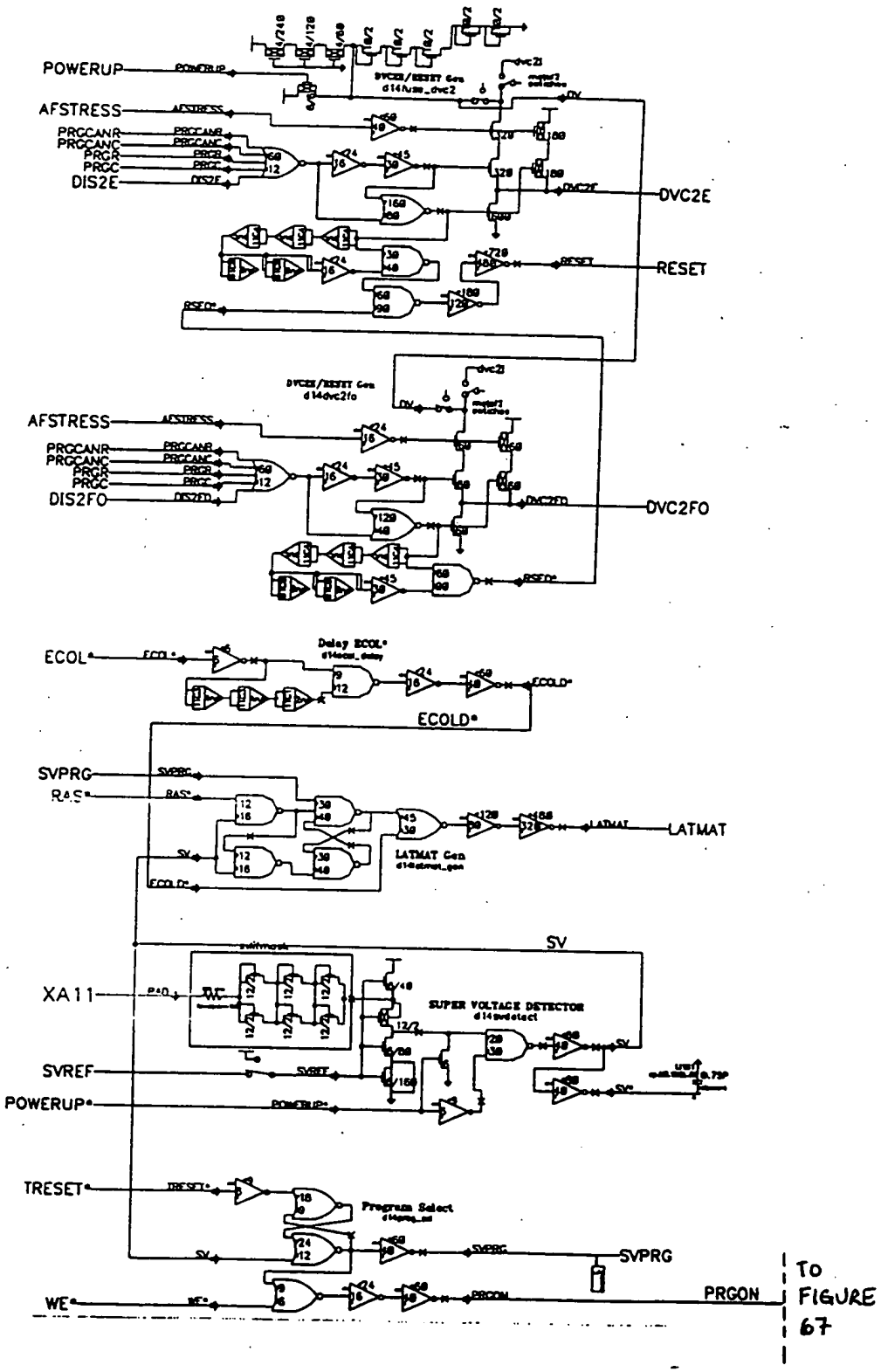


FIGURE 66

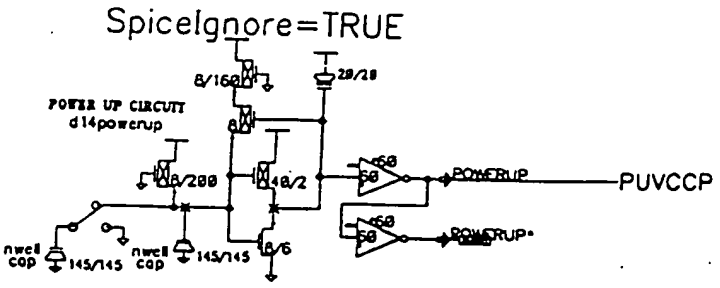


FIGURE 68

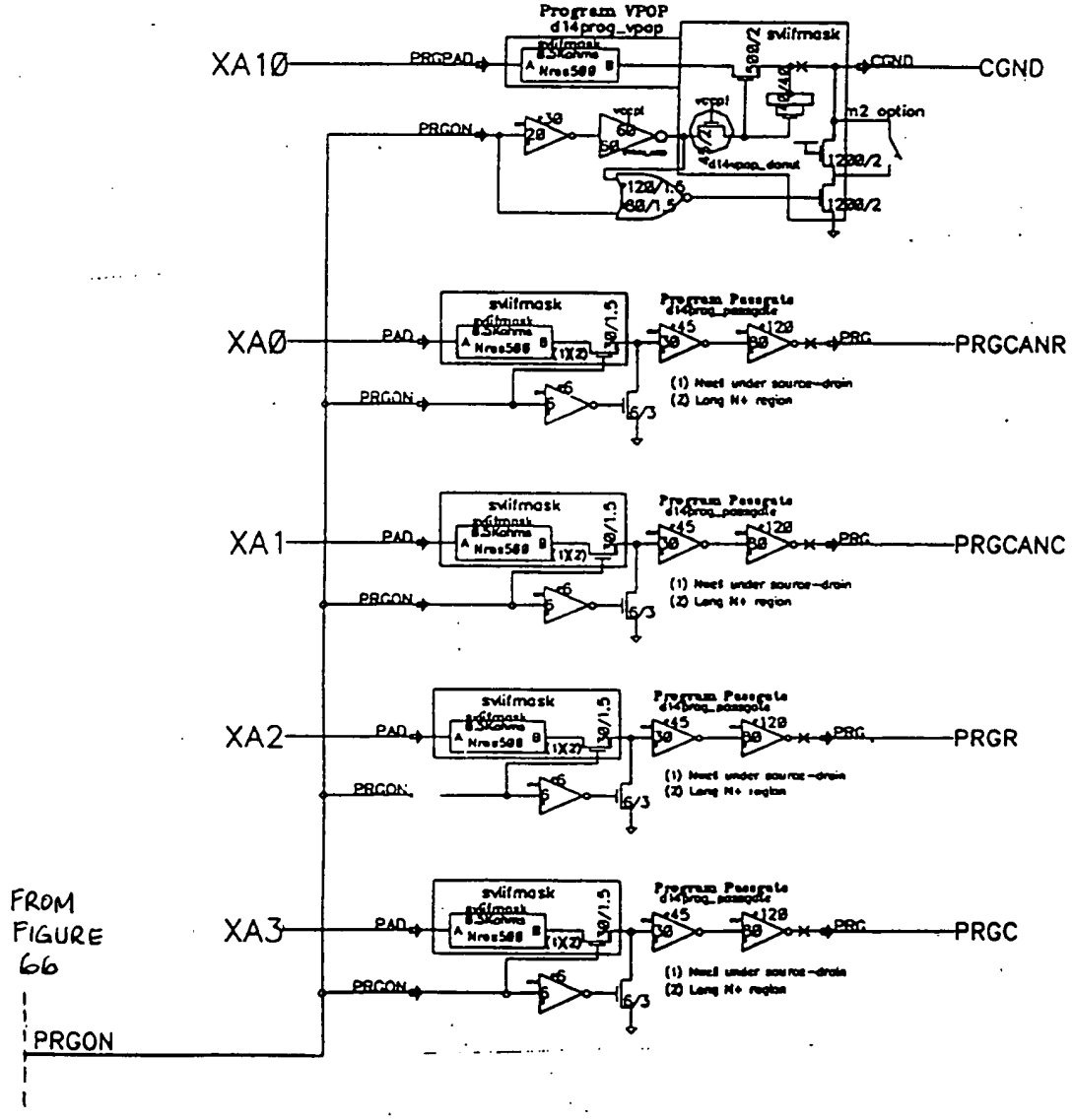


FIGURE 67

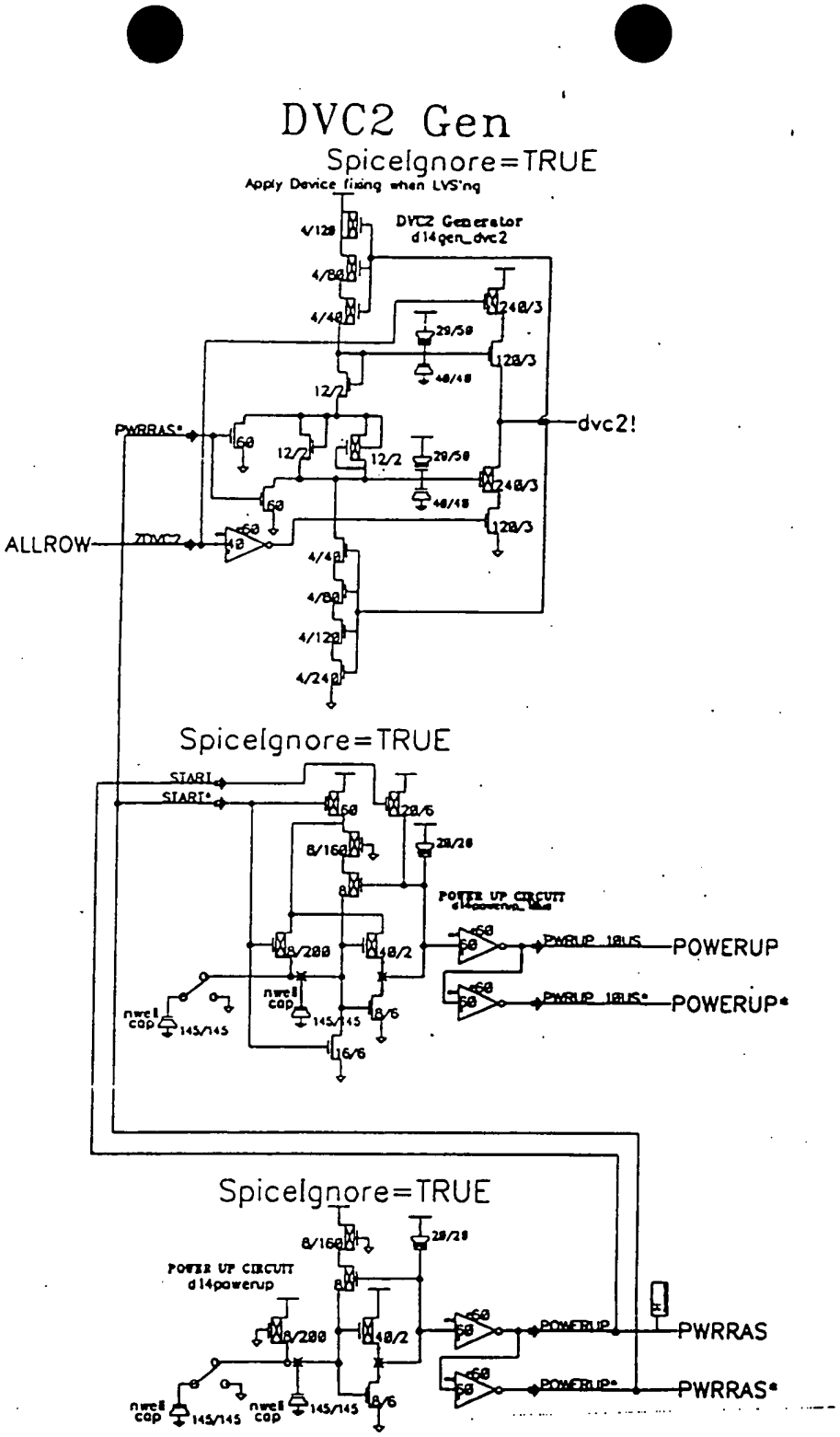

DVC2 Gen
SpiceIgnore=TRUE
Apply Device fixing when LVS'ing
DVC2 Generator
d14gen_dvc2
dvc2!
PWRRAS*
ALLROW
SpiceIgnore=TRUE
START
START*
POWER UP CIRCUIT
POWERUP
POWERUP*
nwell cap
SpiceIgnore=TRUE
POWER UP CIRCUIT
d14powerup
POWERUP
POWERUP*
PWRRAS
PWRRAS*

FIGURE 69

INPUTS OUTPUTS

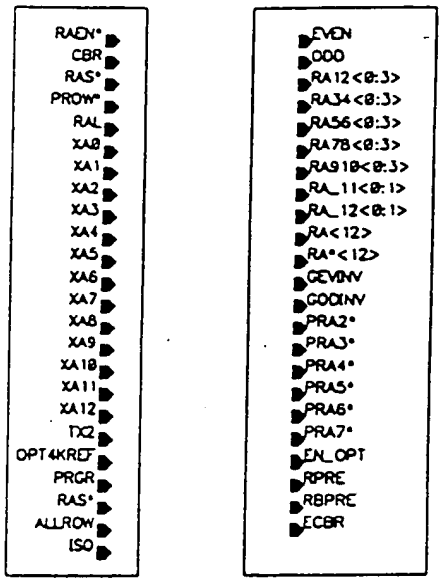


FIGURE 7D

CBR COUNTER

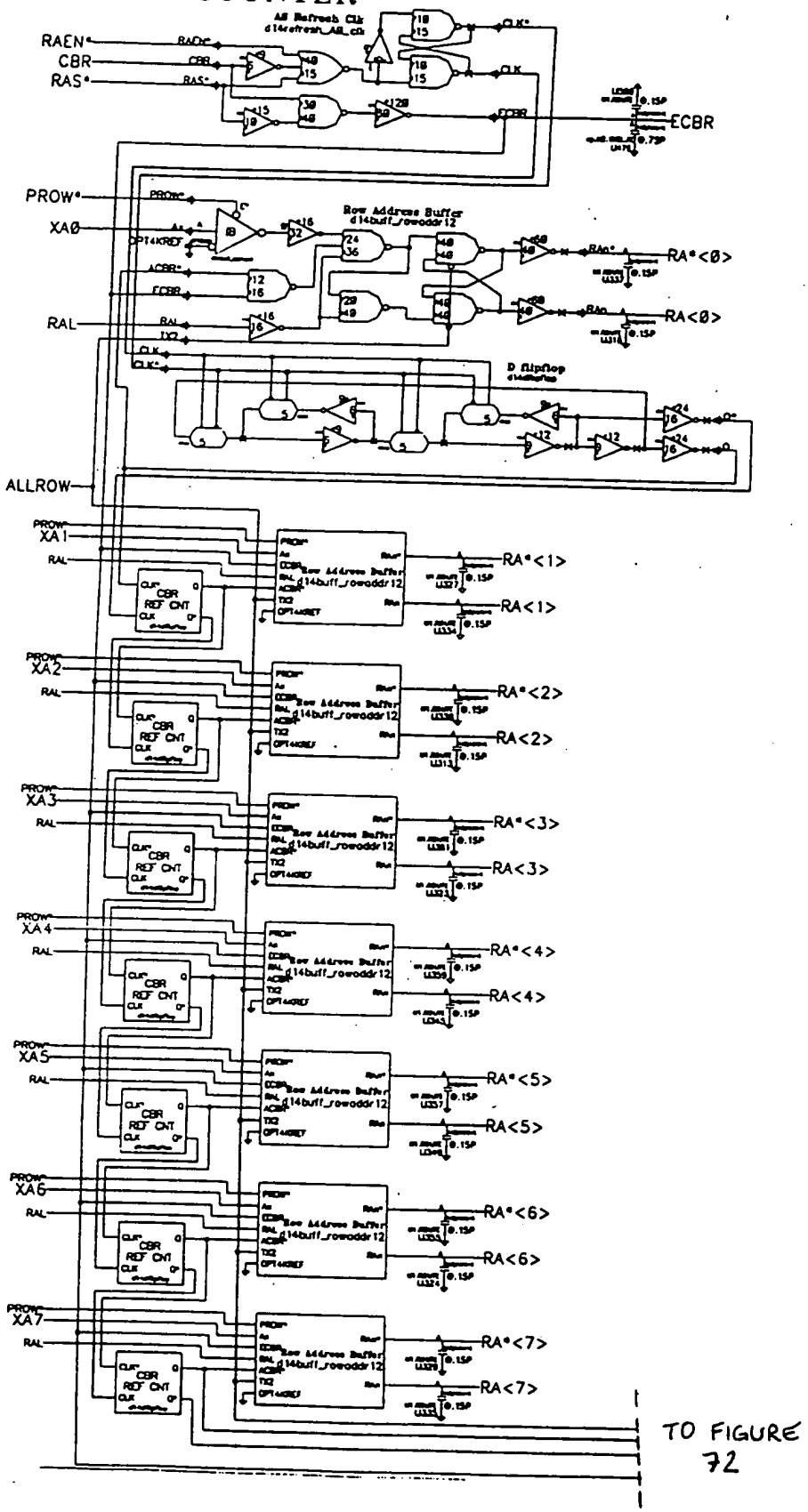


FIGURE 71

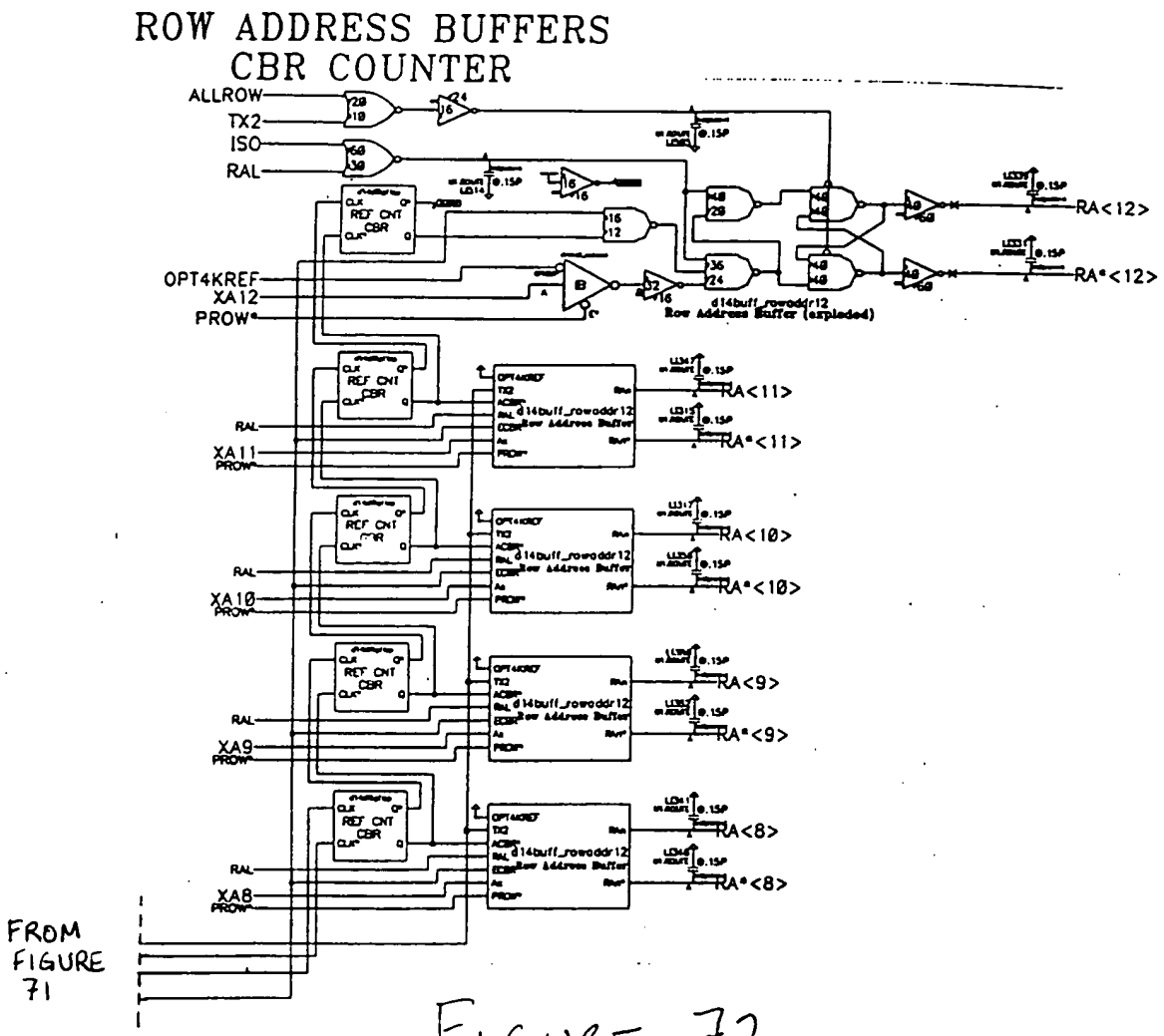


FIGURE 72

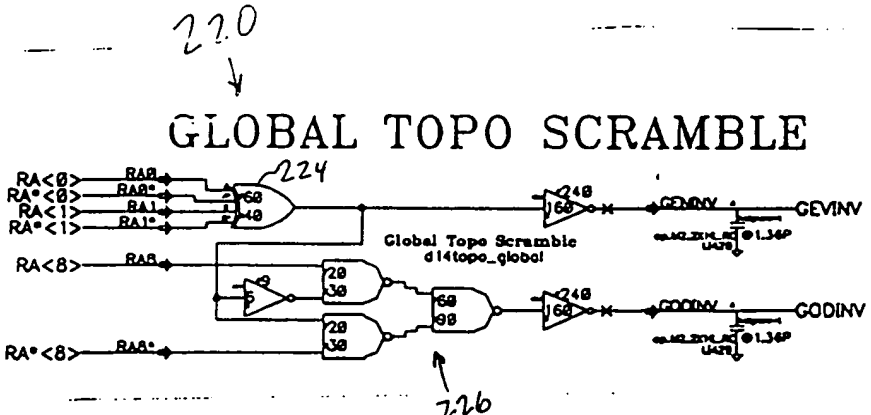


FIGURE 73

FUSE ID ADDRESS

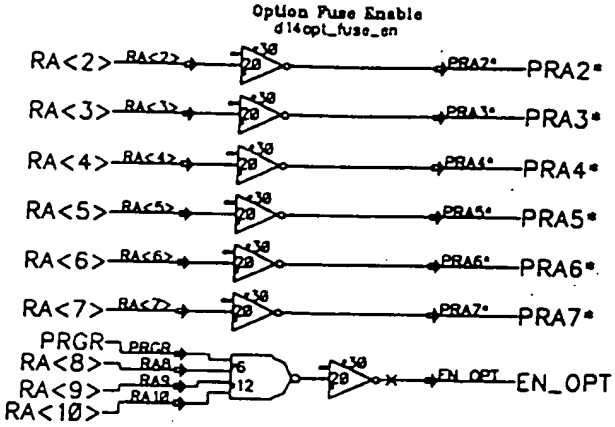


FIGURE 74

RPRE*/RBPRE* GEN

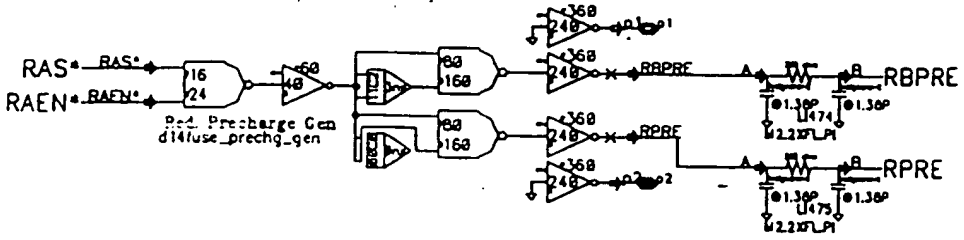


FIGURE 75

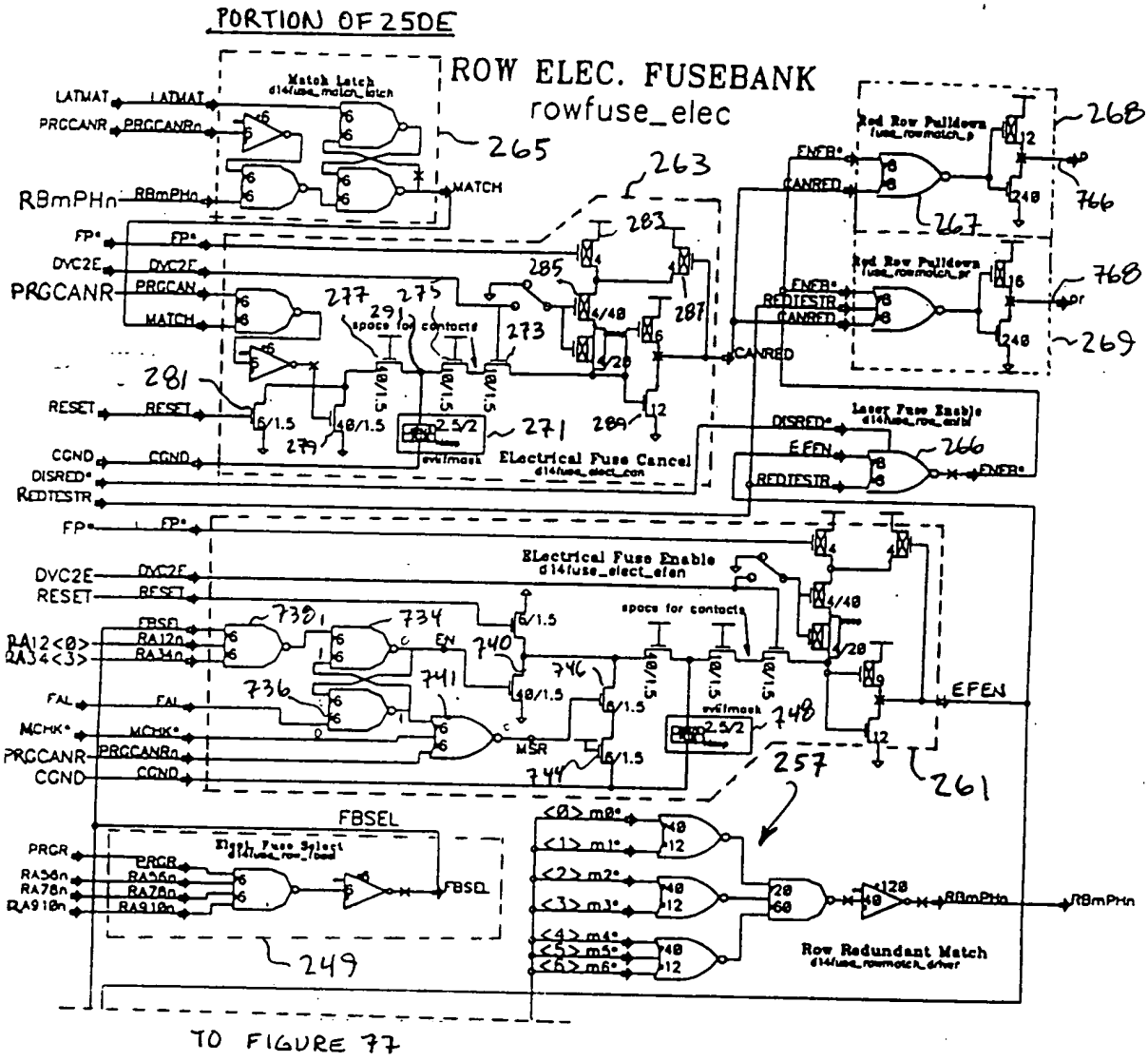

PORTION OF 25DE
ROW ELEC. FUSEBANK
rowfuse_elec
265
263
Match Latch
d14fuse_match_latch
LATMAT
PRGCANR
RBmPHn
MATCH
FP*
DVC2E
PRGCAN
RESET
CGND
DISRED*
REDTESTR
277
275
291
space for contacts
273
285
283
287
281
279
271
289
Electrical Fuse Cancel
d14fuse_elect_can
2.5/2
evelmask
CANRED
Red Row Pulldown
fuse_rowmatch_p
268
267
766
ENFB*
Red Row Pulldown
fuse_rowmatch_pr
768
269
Laser Fuse Enable
d14fuse_row_enbl
266
EFEN
ENFB*
Electrical Fuse Enable
d14fuse_elect_efen
DVC2E
RESET
FBSEL
RA12<0>
RA34<3>
FAL
MCHK*
PRGCANR
CGND
7301
734
EN
740
741
736
746
748
MSR
744
space for contacts
EFEN
257
261
FBSEL
Eight Fuse Select
d14fuse_row_fbsel
PRGR
RA56n
RA78n
RA910n
249
<0> m0*
<1> m1*
<2> m2*
<3> m3*
<4> m4*
<5> m5*
<6> m6*
Row Redundant Match
d14fuse_rowmatch_driver
RBmPHn
TO FIGURE 77

FIGURE 76

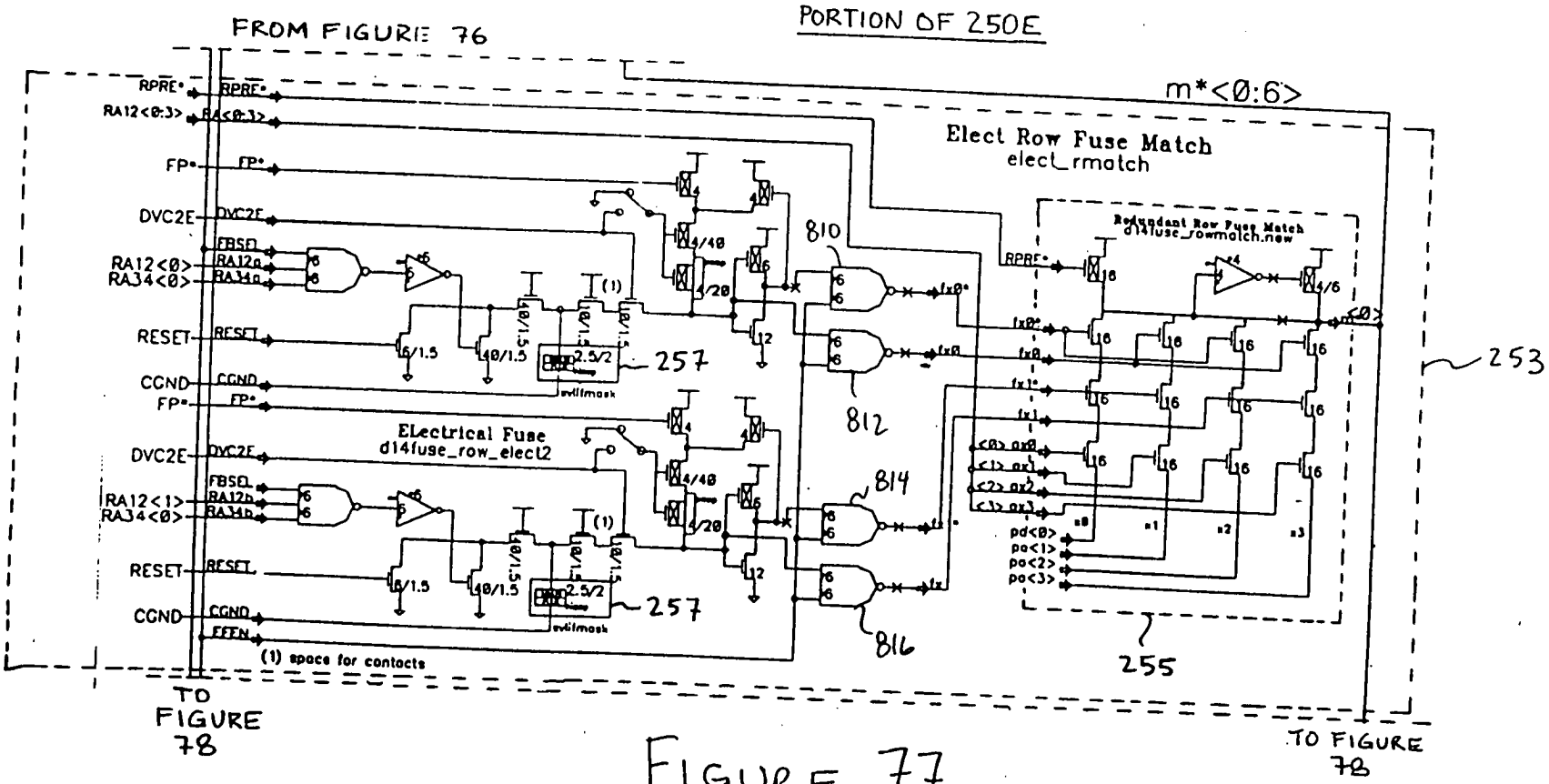

FROM FIGURE 76
PORTION OF 250E
m*<0:6>
Elect Row Fuse Match
elect_rmatch
Redundant Row Fuse Match
d14fuse_rowmatch.new
ELectrical Fuse
d14fuse_row_elect2
RPRE*
RA12<0:3>
FP*
DVC2E
RA12<0>
RA34<0>
RESET
CGND
RA12<1>
RA34<1>
FFEN
810
812
814
816
257
253
255
(1) space for contacts
TO FIGURE 78
TO FIGURE 78

FIGURE 77

250L

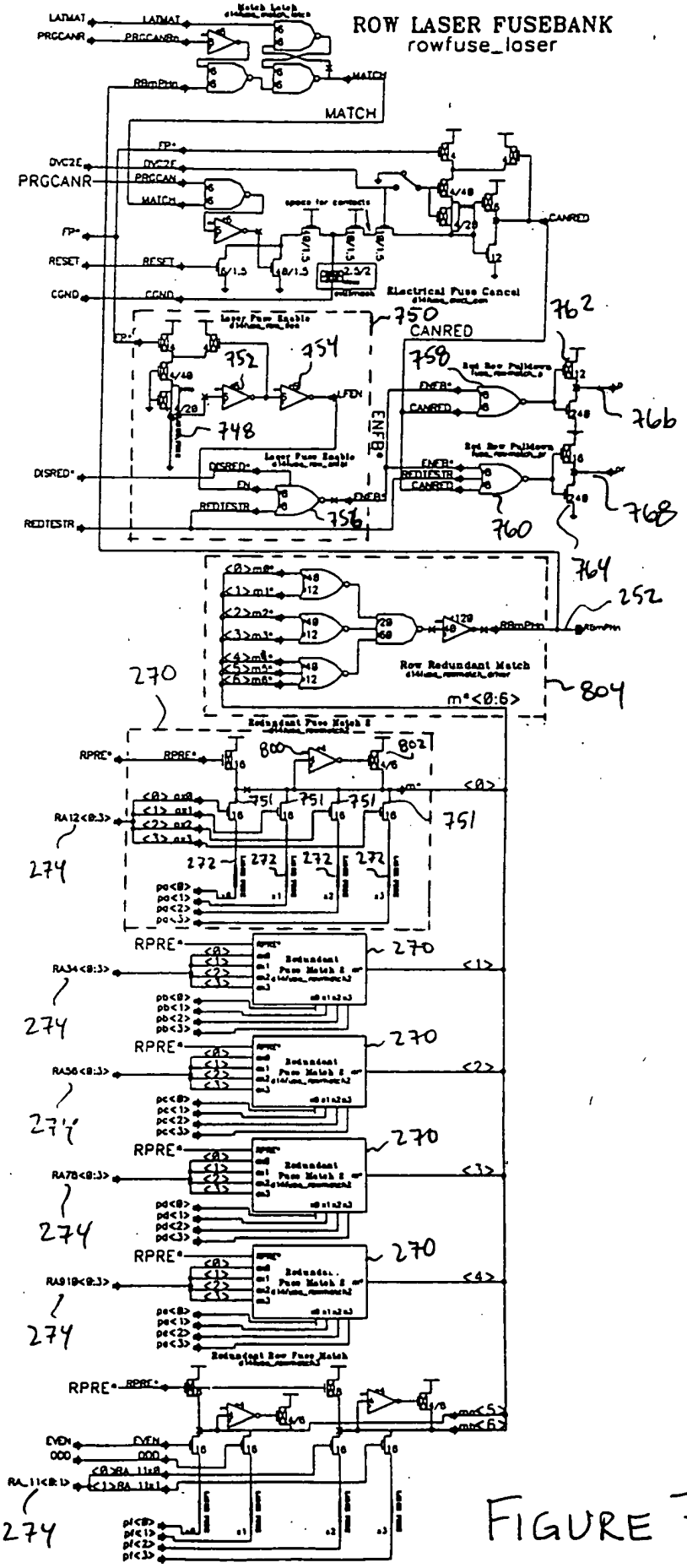


FIGURE 79

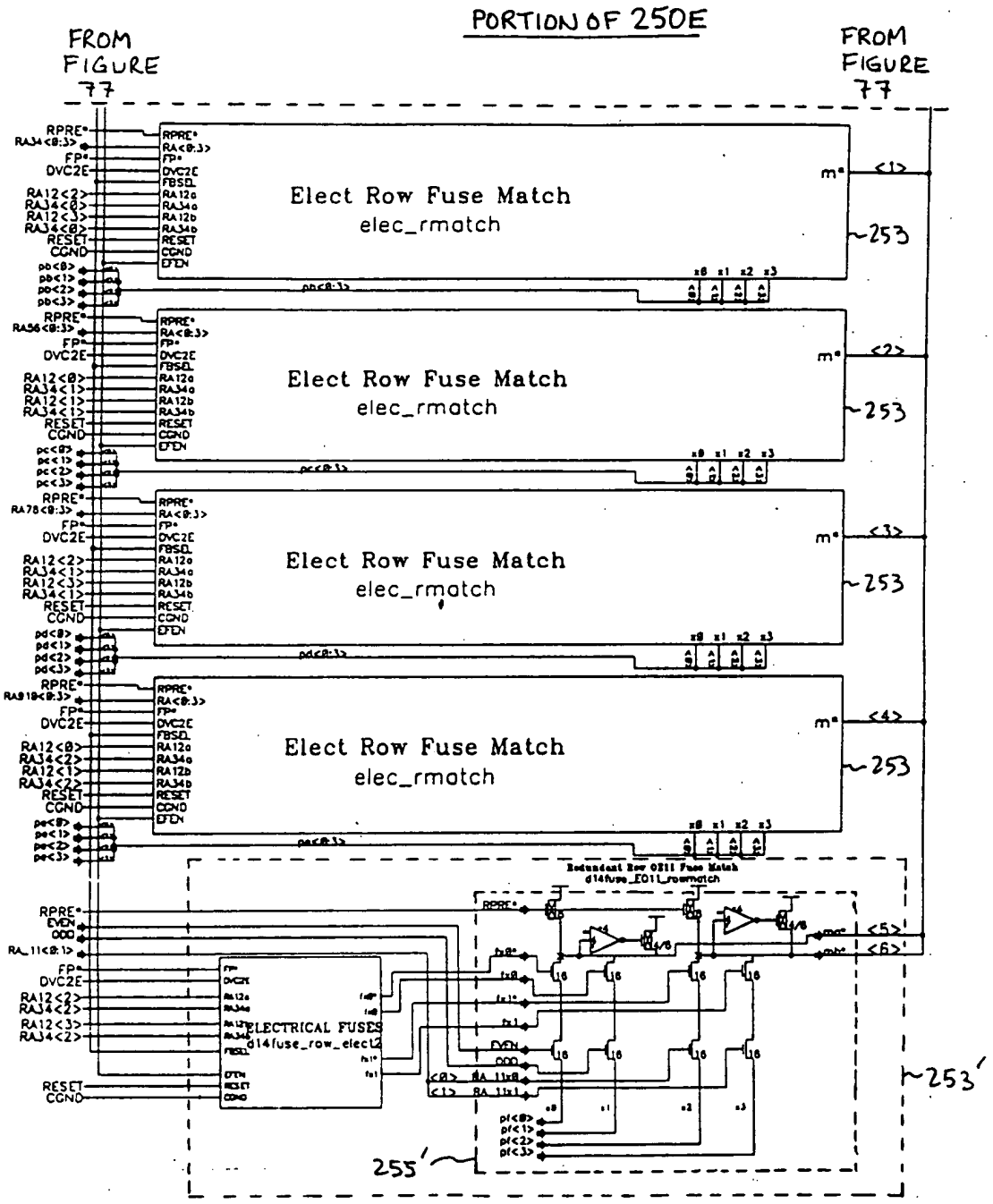

PORTION OF 250E
FROM FIGURE 77
FROM FIGURE 77
Elect Row Fuse Match
elec_rmatch
253
Elect Row Fuse Match
elec_rmatch
253
Elect Row Fuse Match
elec_rmatch
253
Elect Row Fuse Match
elec_rmatch
253
ELECTRICAL FUSES
d14fuse_row_elect2
253'
255'

FIGURE 78

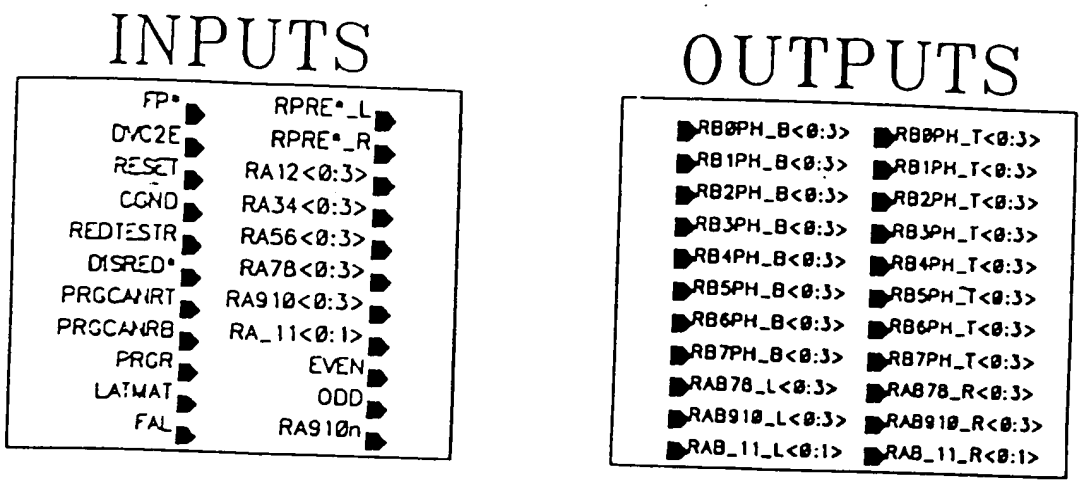

INPUTS
FP*
DVC2E
RESET
CGND
REDTESTR
DISRED*
PRGCANRT
PRGCANRB
PRGR
LATMAT
FAL
RPRE*_L
RPRE*_R
RA12<0:3>
RA34<0:3>
RA56<0:3>
RA78<0:3>
RA910<0:3>
RA_11<0:1>
EVEN
ODD
RA910n
OUTPUTS
RB0PH_B<0:3>
RB1PH_B<0:3>
RB2PH_B<0:3>
RB3PH_B<0:3>
RB4PH_B<0:3>
RB5PH_B<0:3>
RB6PH_B<0:3>
RB7PH_B<0:3>
RAB78_L<0:3>
RAB910_L<0:3>
RAB_11_L<0:1>
RB0PH_T<0:3>
RB1PH_T<0:3>
RB2PH_T<0:3>
RB3PH_T<0:3>
RB4PH_T<0:3>
RB5PH_T<0:3>
RB6PH_T<0:3>
RB7PH_T<0:3>
RAB78_R<0:3>
RAB910_R<0:3>
RAB_11_R<0:1>

FIGURE 80

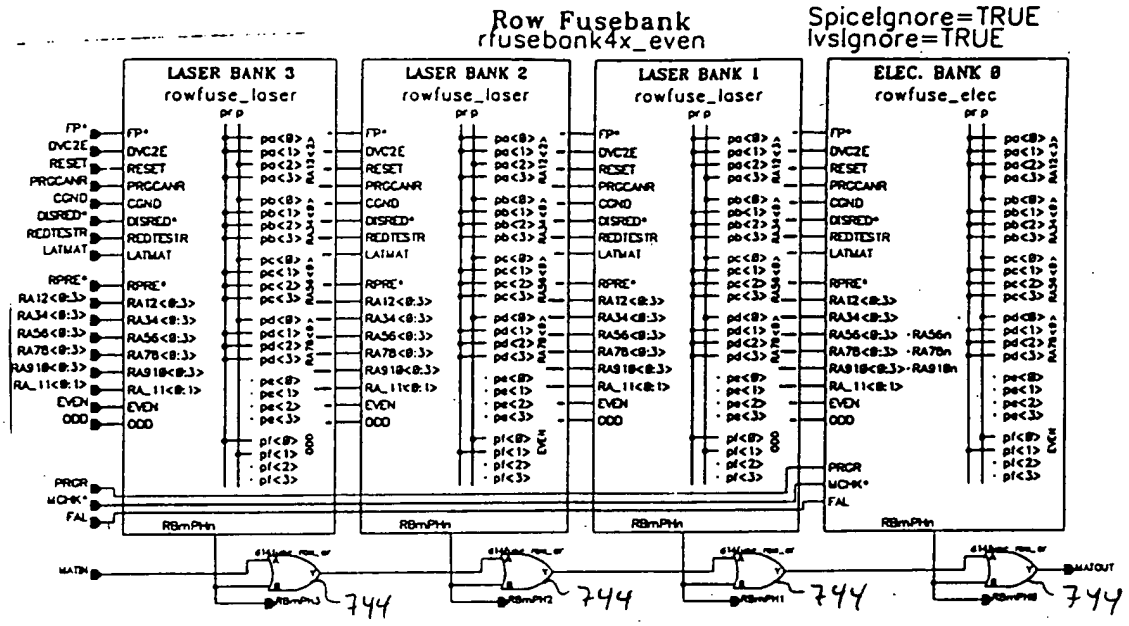


FIGURE 81

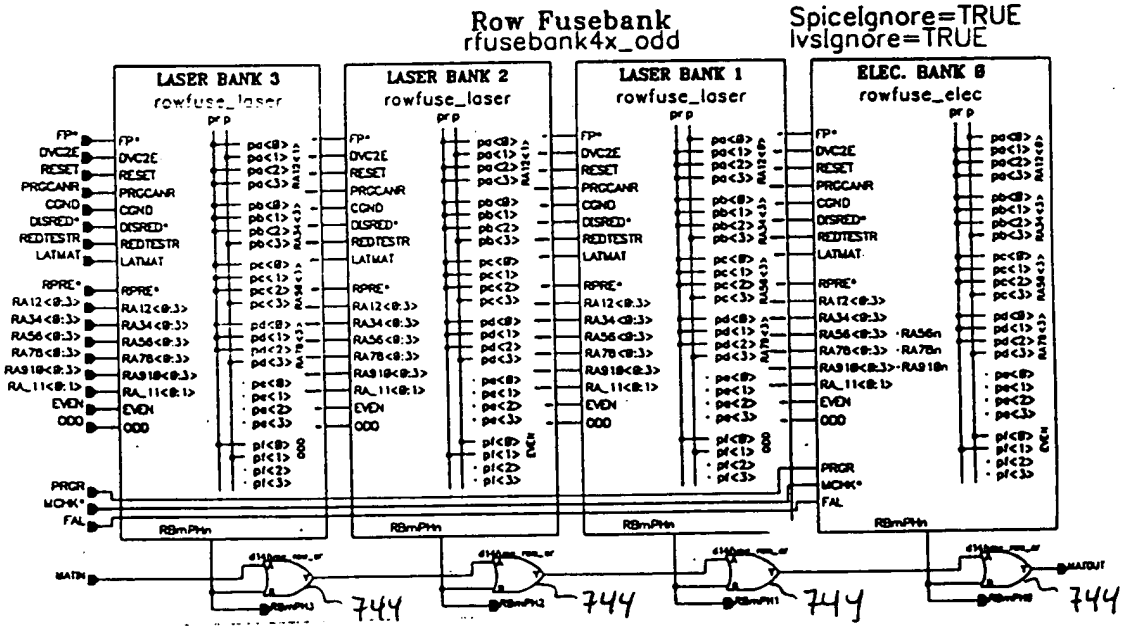


FIGURE 82

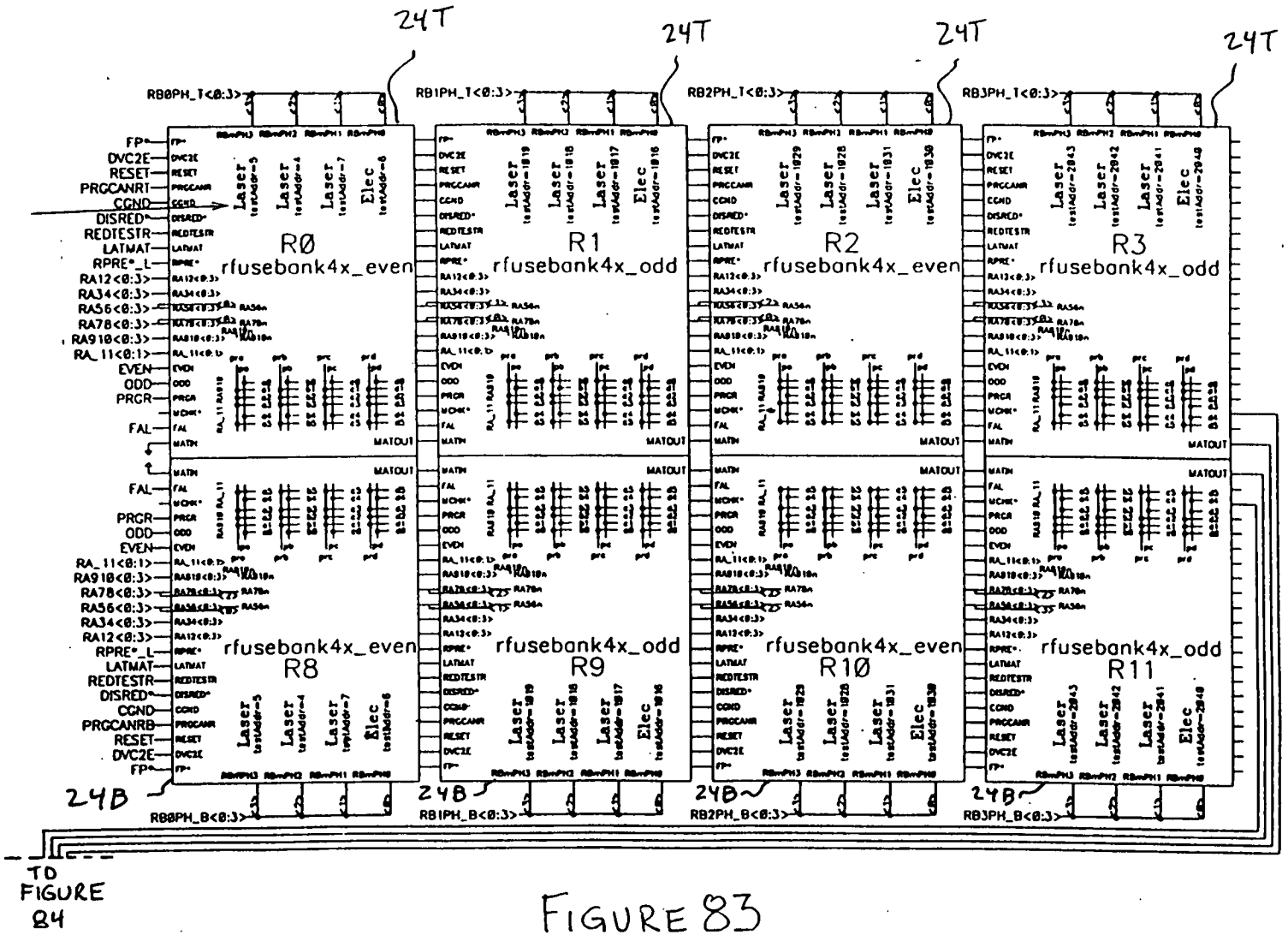

24T
24T
24T
24T
RB0PH_T<0:3>
RB1PH_T<0:3>
RB2PH_T<0:3>
RB3PH_T<0:3>
FP*
DVC2E
RESET
PRGCANRT
CGND
DISRED*
REDTESTR
LATMAT
RPRE*_L
RA12<0:3>
RA34<0:3>
RA56<0:3>
RA78<0:3>
RA910<0:3>
RA_11<0:1>
EVEN
ODD
PRGR
FAL
MATH
MATOUT
Laser
Elec
R0
rfusebank4x_even
R1
rfusebank4x_odd
R2
rfusebank4x_even
R3
rfusebank4x_odd
R8
rfusebank4x_even
R9
rfusebank4x_odd
R10
rfusebank4x_even
R11
rfusebank4x_odd
PRGCANRB
24B
24B
24B
24B
RB0PH_B<0:3>
RB1PH_B<0:3>
RB2PH_B<0:3>
RB3PH_B<0:3>
TO FIGURE 84

FIGURE 83

FROM FIGURE 83

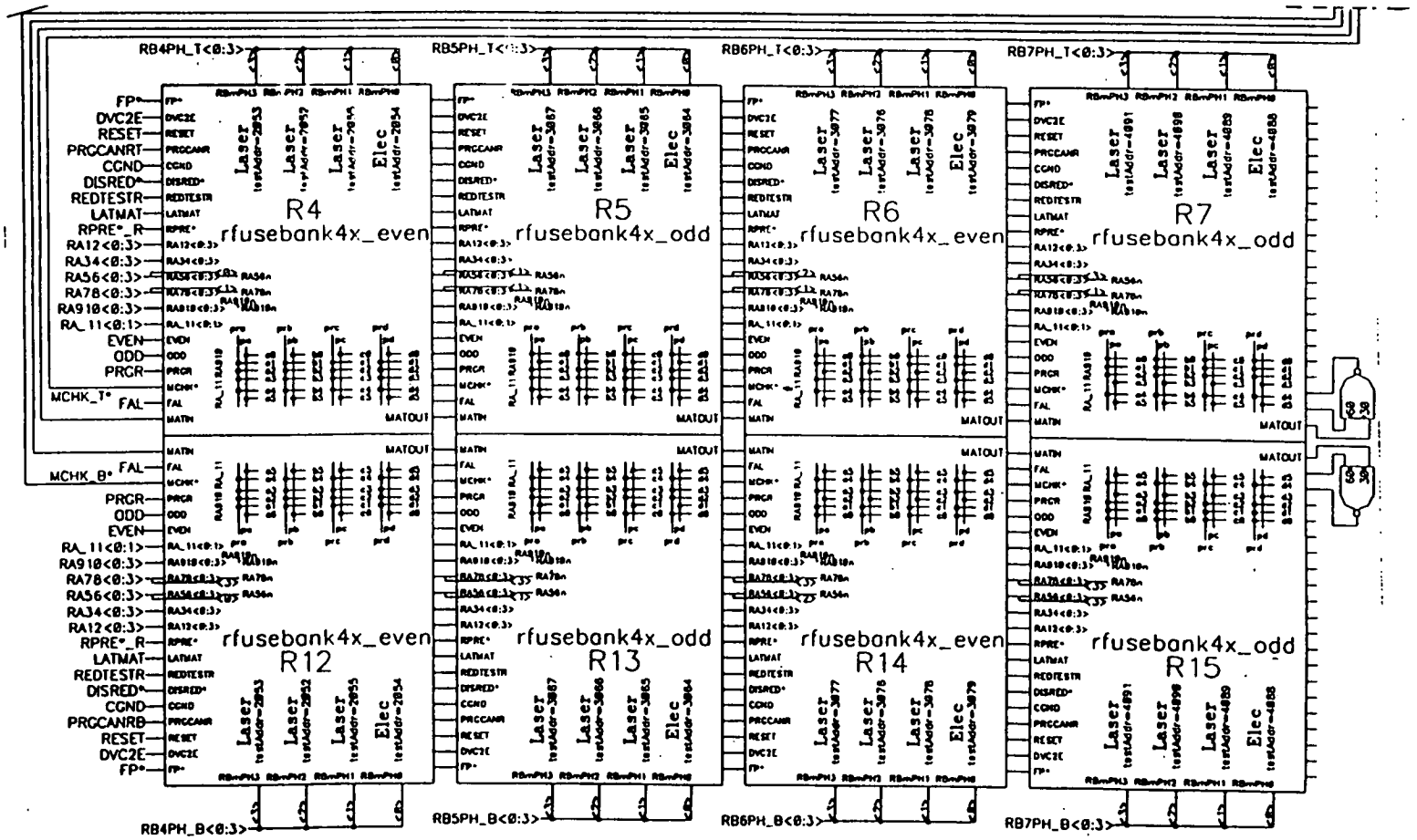


FIGURE 84

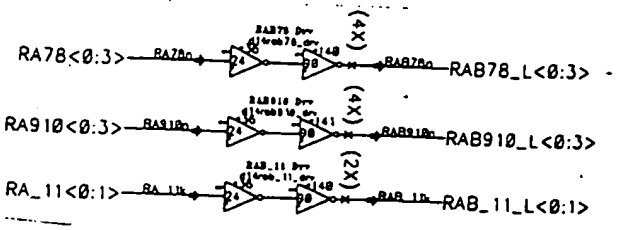


FIGURE 85

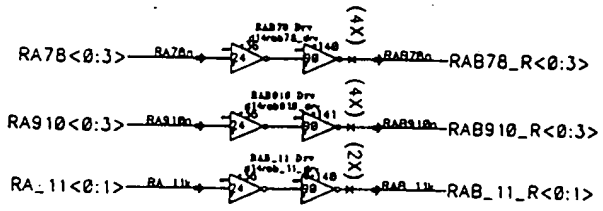


FIGURE 86

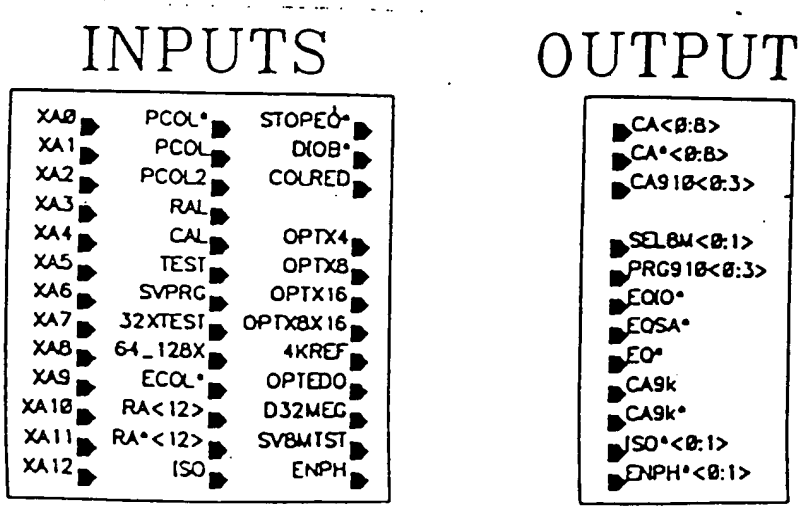

INPUTS
OUTPUTS
XA0
XA1
XA2
XA3
XA4
XA5
XA6
XA7
XA8
XA9
XA10
XA11
XA12
PCOL*
PCOL
PCOL2
RAL
CAL
TEST
SVPRG
32XTEST
64_128X
ECOL*
RA<12>
RA*<12>
ISO
STOPEO*
DIOB*
COLRED
OPTX4
OPTX8
OPTX16
OPTX8X16
4KREF
OPTEDO
D32MEG
SV8MTST
ENPH
CA<0:8>
CA*<0:8>
CA910<0:3>
SEL8M<0:1>
PRG910<0:3>
EOIO*
EOSA*
EO*
CA9k
CA9k*
ISO*<0:1>
ENPH*<0:1>

FIGURE 87

COLUMN ADDRESS BUFFERS/ATD

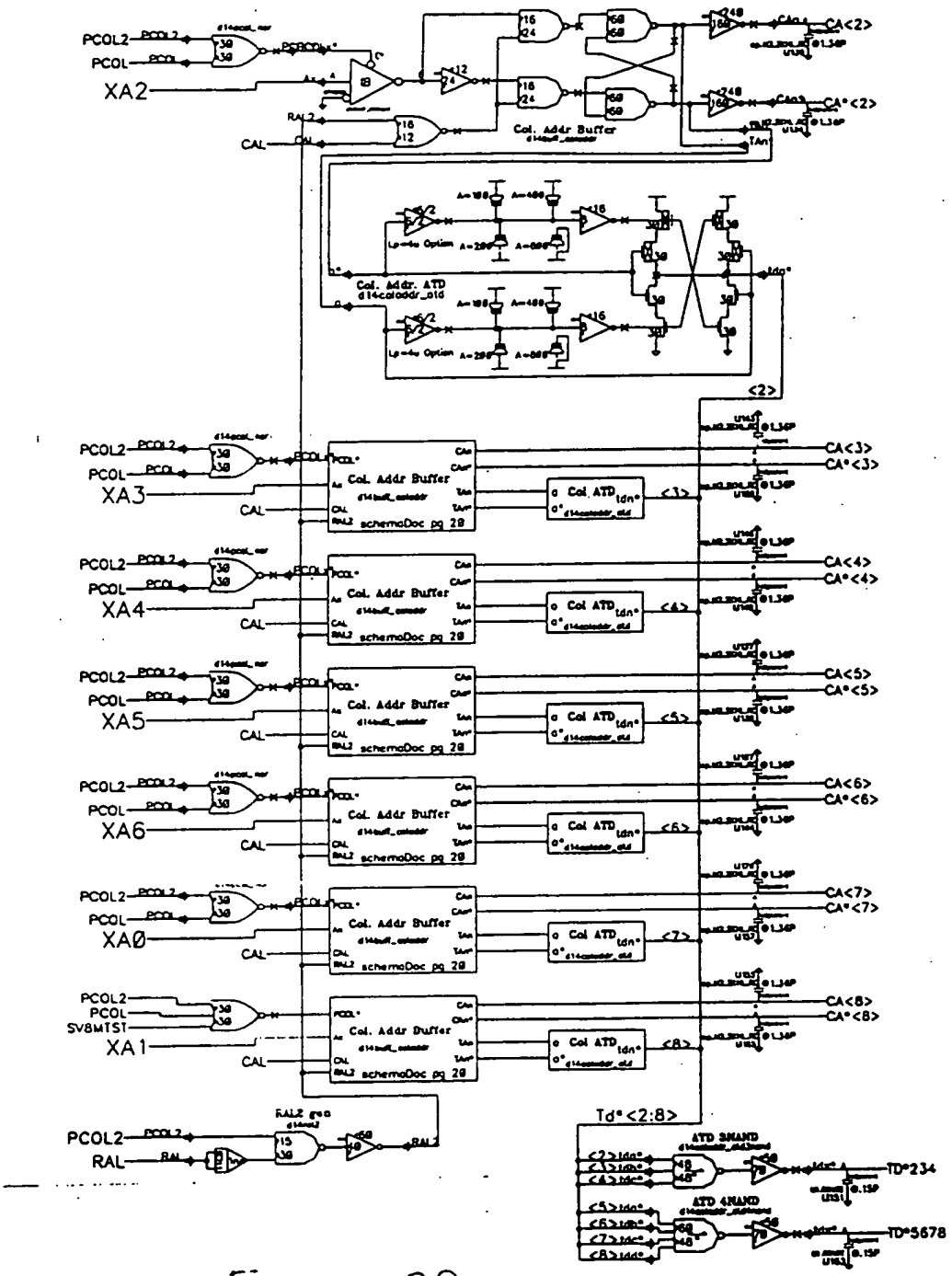


FIGURE 89

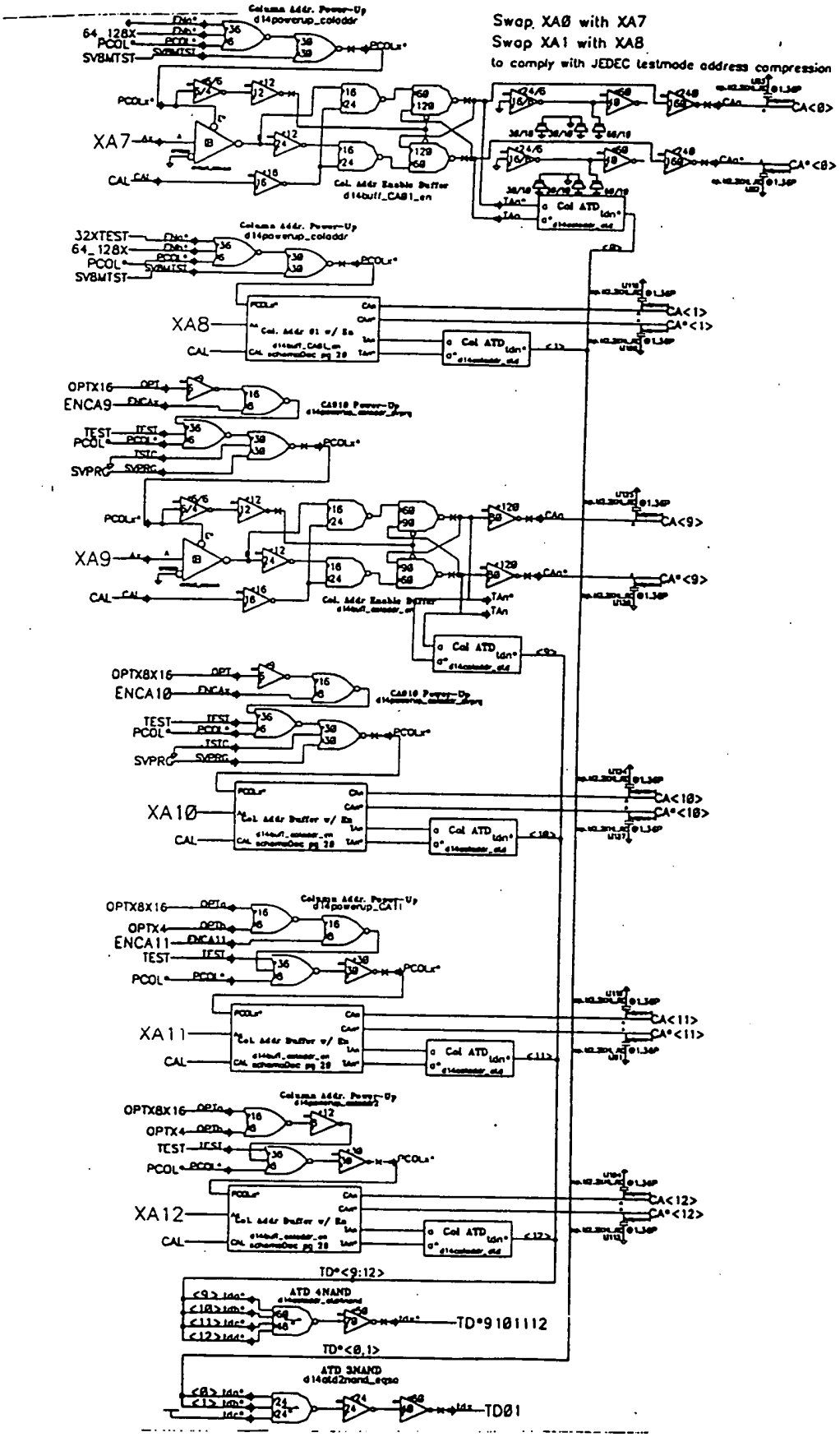

Swap XA0 with XA7
Swap XA1 with XA8
to comply with JEDEC testmode address compression
XA7
XA8
XA9
XA10
XA11
XA12
CAL
PCOL
SVBMTST
64_128X
32XTEST
OPTX16
ENCA9
OPTX8X16
ENCA10
OPTX4
ENCA11
TEST
SVPRG
CA<8>
CA*<8>
CA<1>
CA*<1>
CA<9>
CA*<9>
CA<10>
CA*<10>
CA<11>
CA*<11>
CA<12>
CA*<12>
TD*<9:12>
TD*9101112
TD*<0,1>
TD01

FIGURE 90

CONFIG	ROW ADDRESS		COLUMN ADDRESS	
	8K ref	4K ref	8K ref	4K ref
4MX16	A0 – A12	A0 – A11	A0 – A8	A0 – A9
8MX8	A0 – A12	A0 – A11	A0 – A9	A0 – A10
16MX4	A0 – A12	A0 – A11	A0 – A10	A0 – A11
64MX1	A0 – A12	_	A0 – A12	_

Test Mode Address Compression (ref to X1) The following column addresses are ignored	
16X	A12, A11, A10, A9
32X	A12, A11, A10, A9, A8
64X	A12, A11, A10, A9, A8, A7
128X	A12, A11, A10, A9, A8, A7, RA12

FIGURE 88

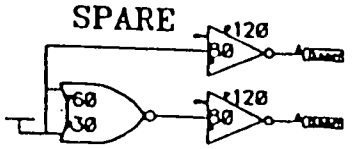


FIGURE 92

4KREF IGNORE

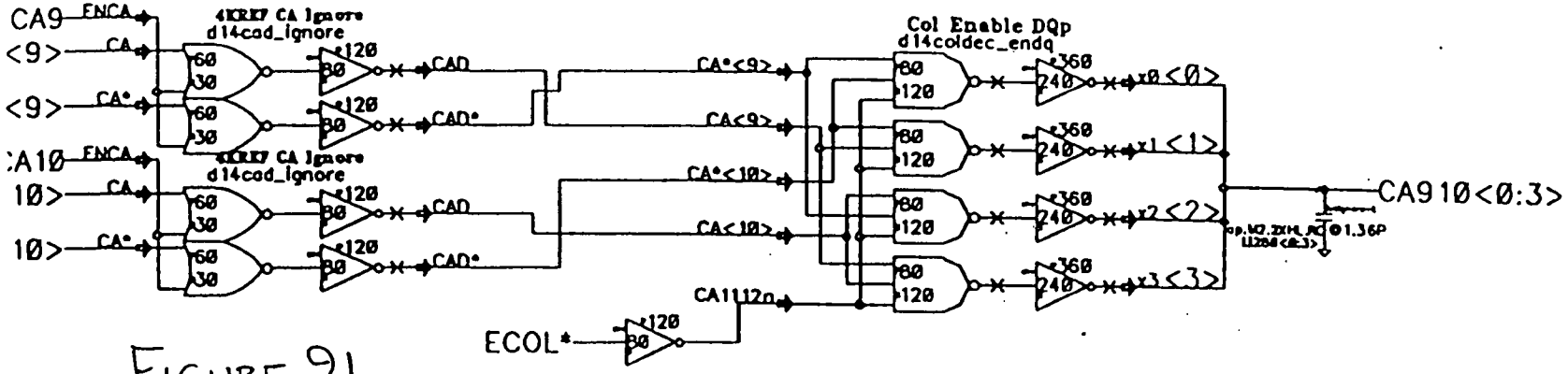


FIGURE 91

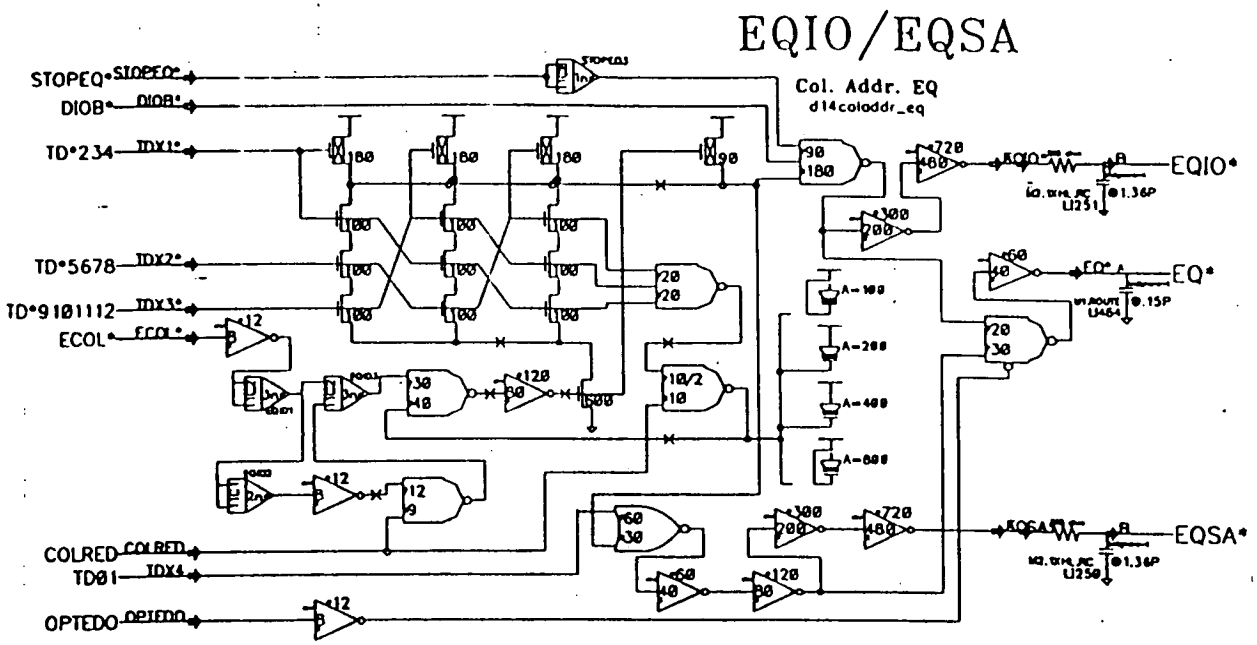

EQIO/EQSA
STOPEQ*
DIOB*
TD*234
TD*5678
TD*9101112
ECOL*
COLRED
TD01
OPTEDO
Col. Addr. EQ
d14coladdr_eq
EQIO*
EQ*
EQSA*

FIGURE 93

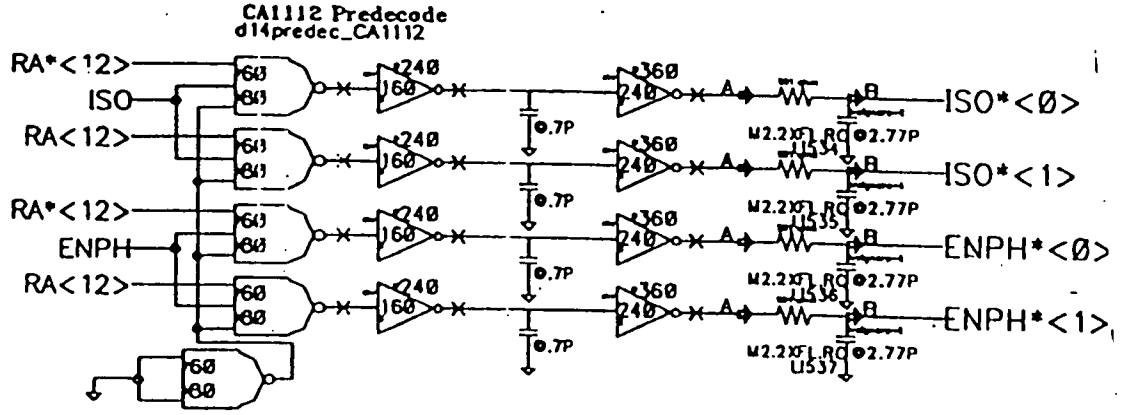

CA1112 Predecode
d14predec_CA1112
RA*<12>
ISO
RA<12>
RA*<12>
ENPH
RA<12>
ISO*<0>
ISO*<1>
ENPH*<0>
ENPH*<1>

FIGURE 94

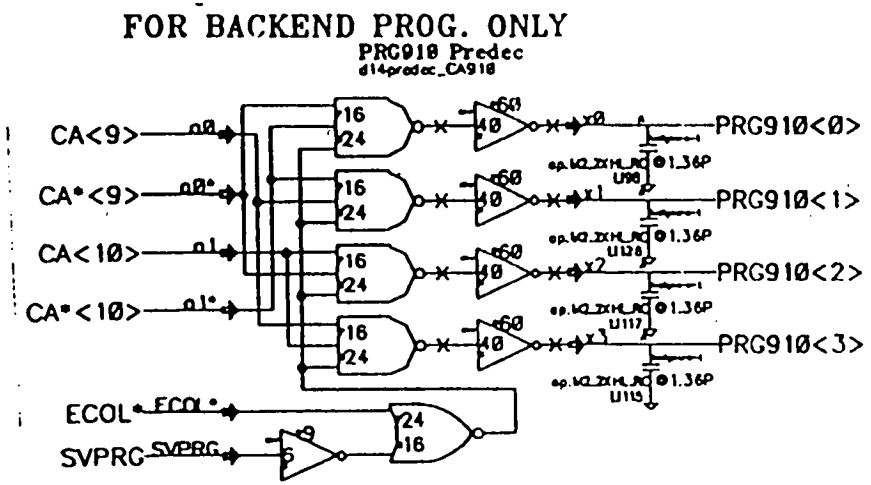


FIGURE 95

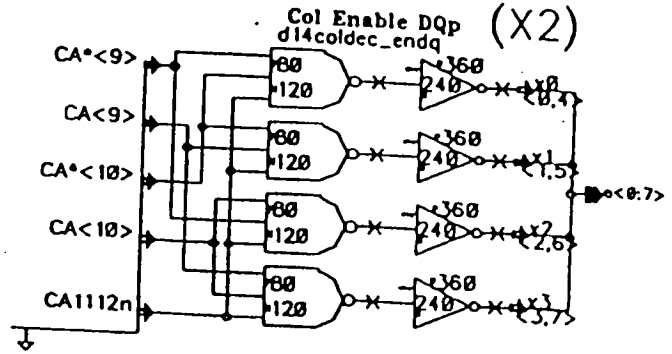


FIGURE 96

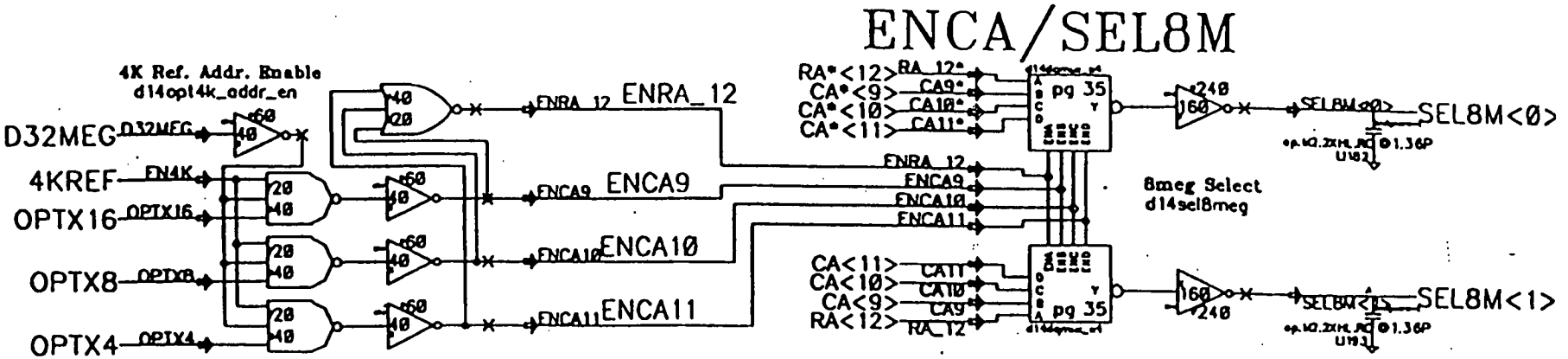


FIGURE 97

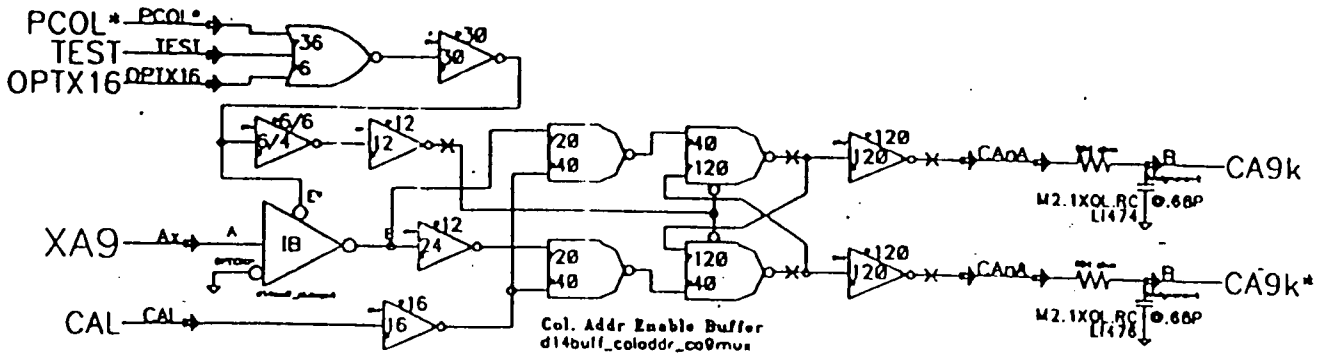

PCOL*
TEST
OPTX16
XA9
CAL
Col. Addr Enable Buffer
d14buff_coloddr_co9mux
CA9k
CA9k*

FIGURE 98

LOCAL ROW DECODE

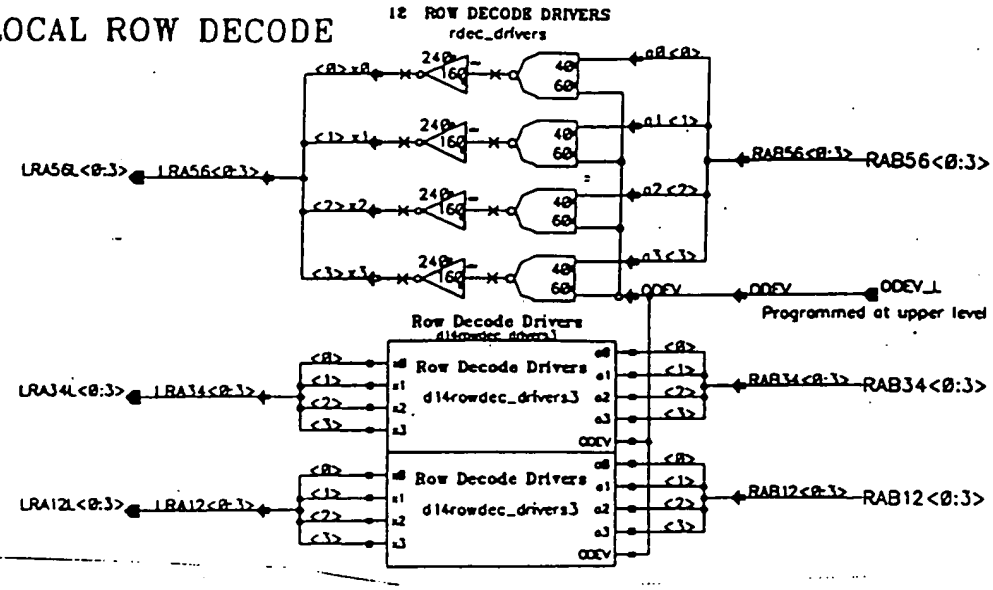


FIGURE 99

COLUMN SELECT

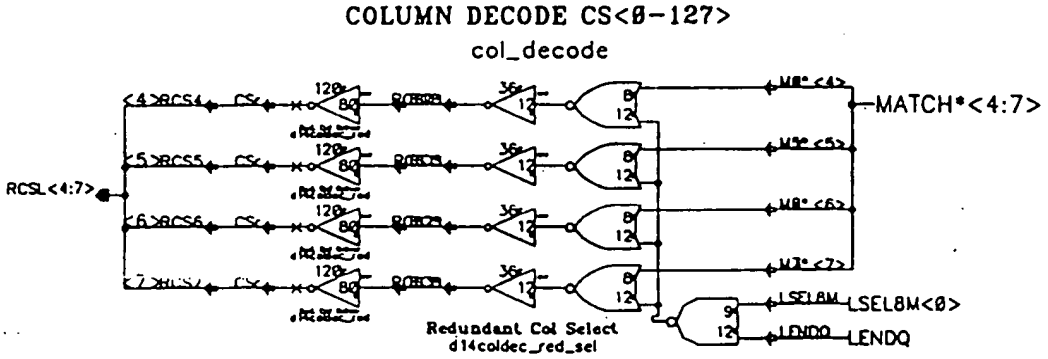


FIGURE 100

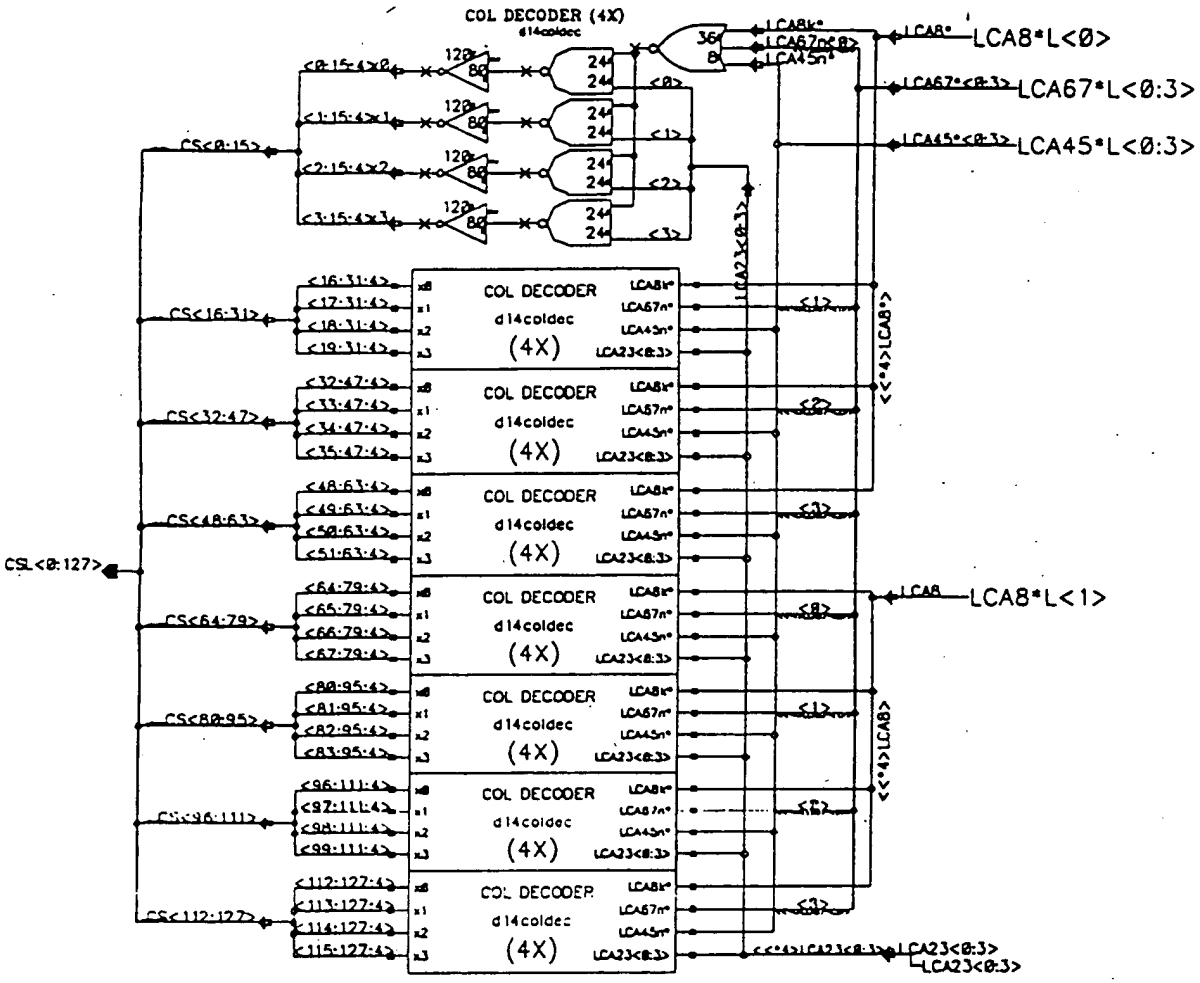

COL DECODER (4X)
d14coldec
CSL<0:127>
CS<0:15>
CS<16:31>
CS<32:47>
CS<48:63>
CS<64:79>
CS<80:95>
CS<96:111>
CS<112:127>
COL DECODER
d14coldec
(4X)
LCA8*L<0>
LCA67*L<0:3>
LCA45*L<0:3>
LCA8*L<1>
LCA23<0:3>

FIGURE 101

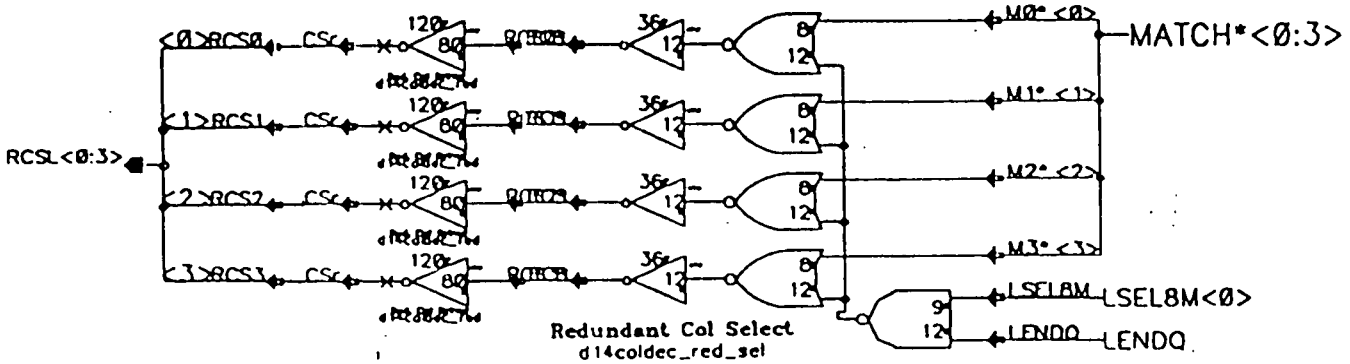

RCSL<0:3>
<0>RCS0
<1>RCS1
<2>RCS2
<3>RCS3
CSc
120
80
36
12
8
12
9
12
M0*<0>
M1*<1>
M2*<2>
M3*<3>
MATCH*<0:3>
LSEL8M
LSEL8M<0>
LENDQ
LENDQ
Redundant Col Select
d14coldec_red_sel

FIGURE 102

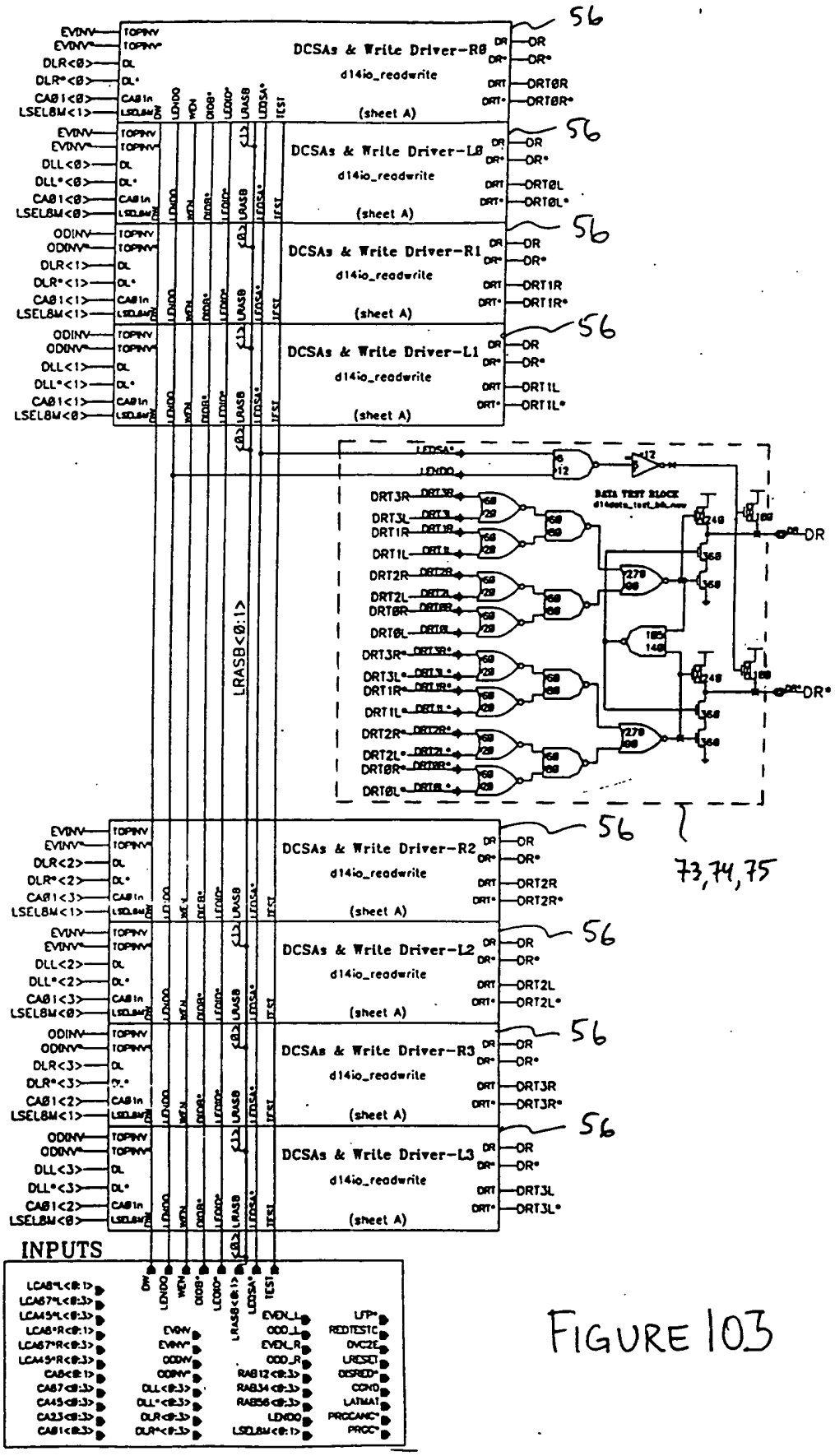

DCSAs & Write Driver-R0
DCSAs & Write Driver-L0
DCSAs & Write Driver-R1
DCSAs & Write Driver-L1
DCSAs & Write Driver-R2
DCSAs & Write Driver-L2
DCSAs & Write Driver-R3
DCSAs & Write Driver-L3
d14io_readwrite
(sheet A)
56
LRASB<0:1>
DRT3R
DRT3L
DRT1R
DRT1L
DRT2R
DRT2L
DRT0R
DRT0L
DR
DR*
73,74,75
INPUTS

FIGURE 103

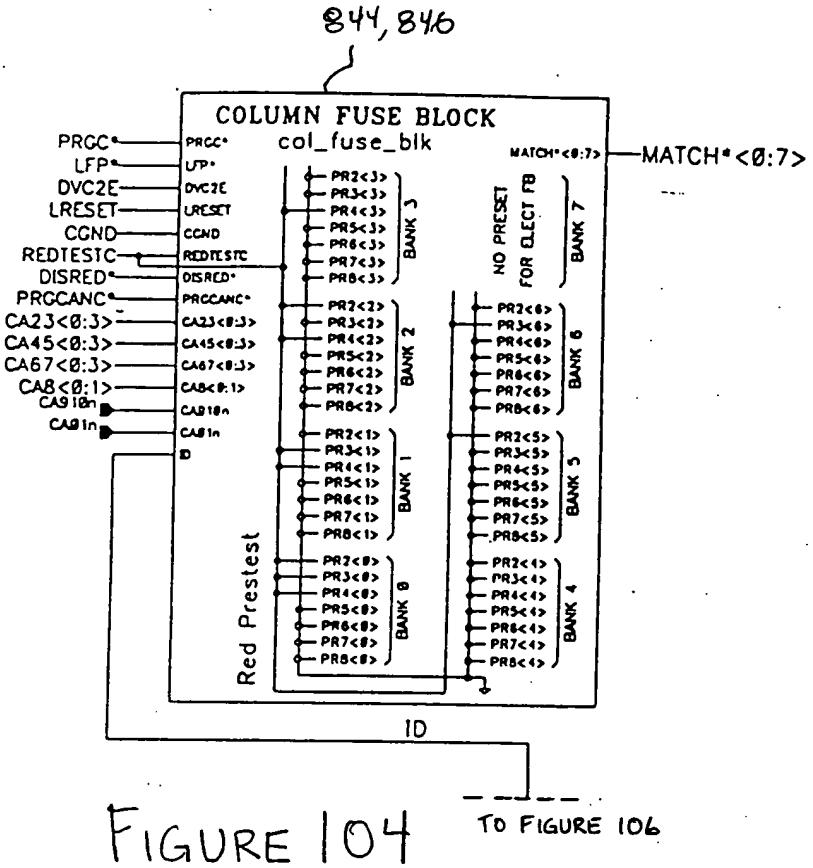


FIGURE 104

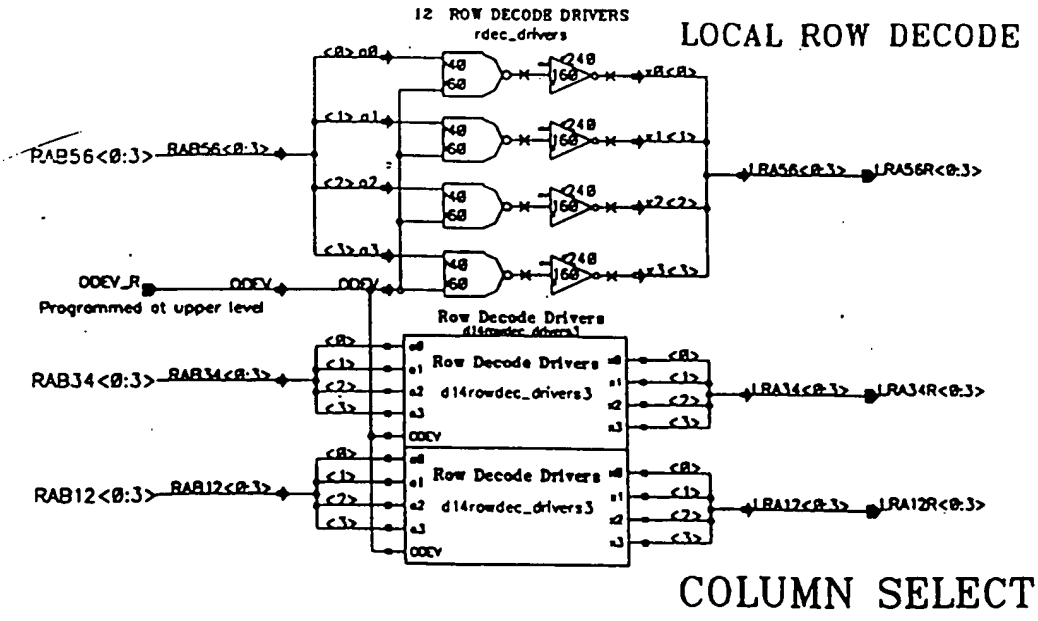


FIGURE 105

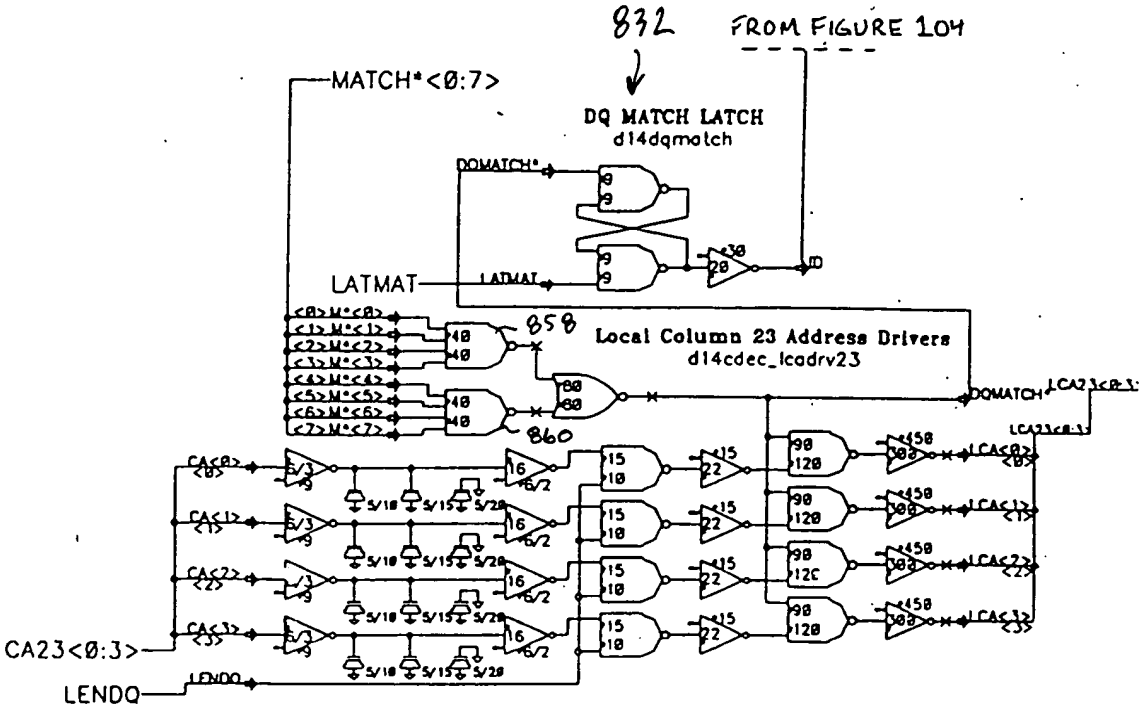


FIGURE 106

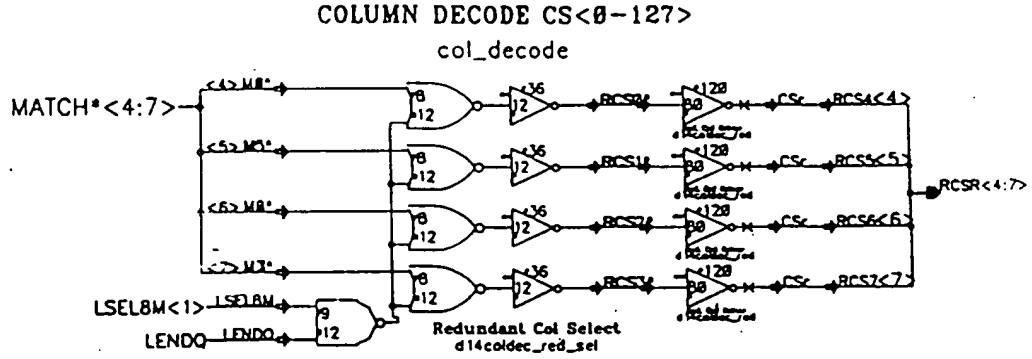


FIGURE 107

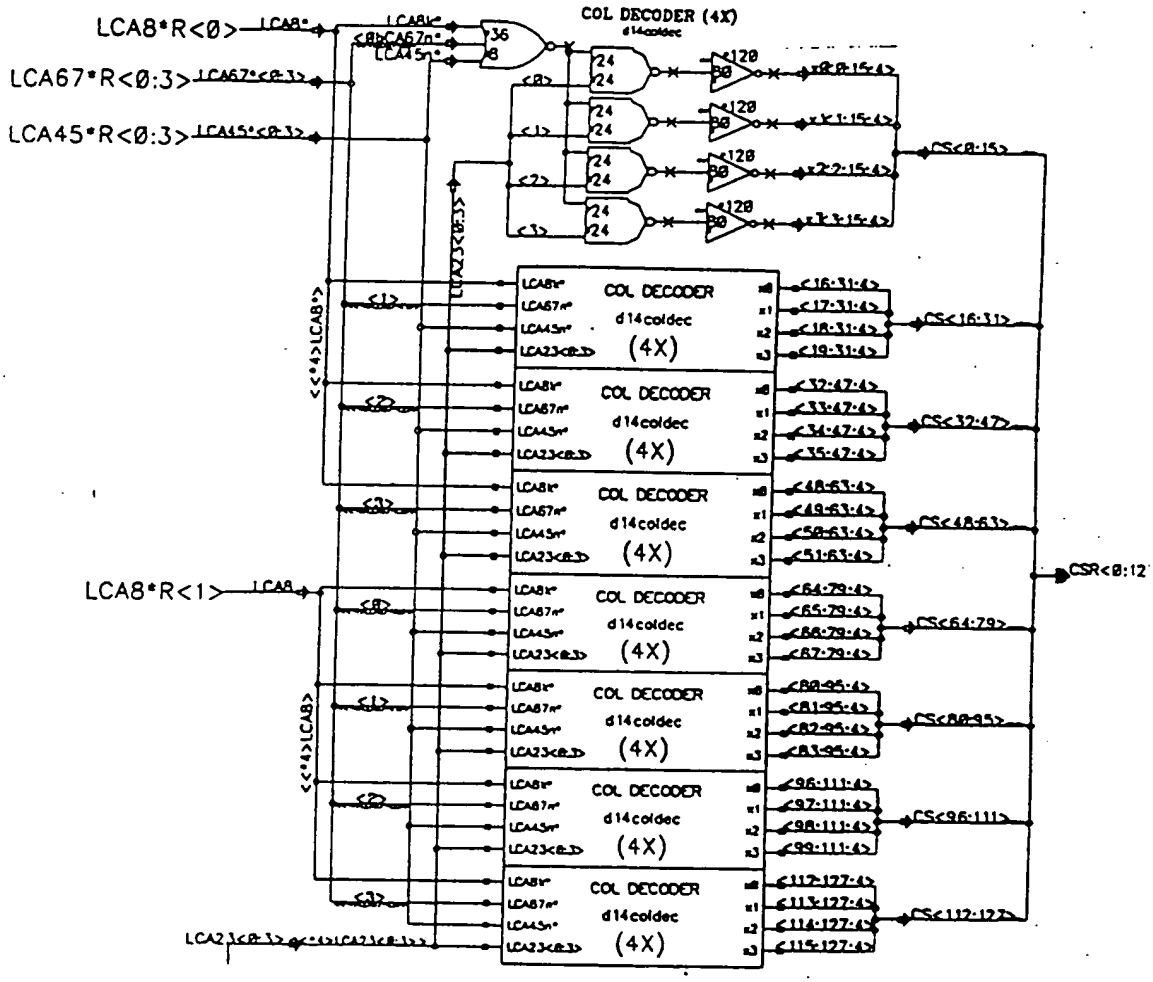


FIGURE 108

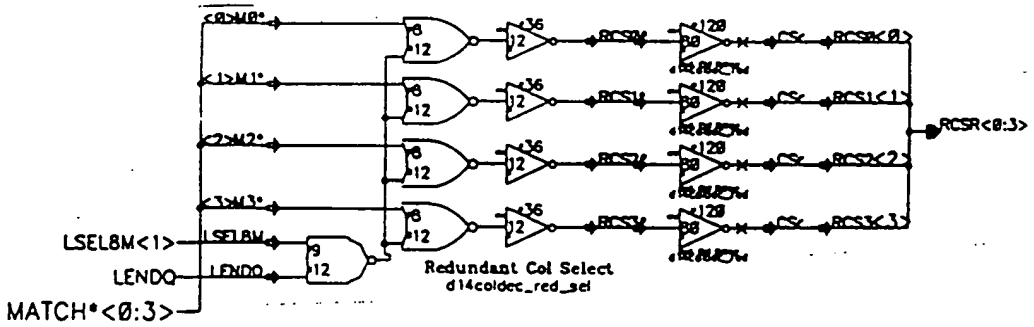


FIGURE 109

SEVEN LASER FUSE BANKS

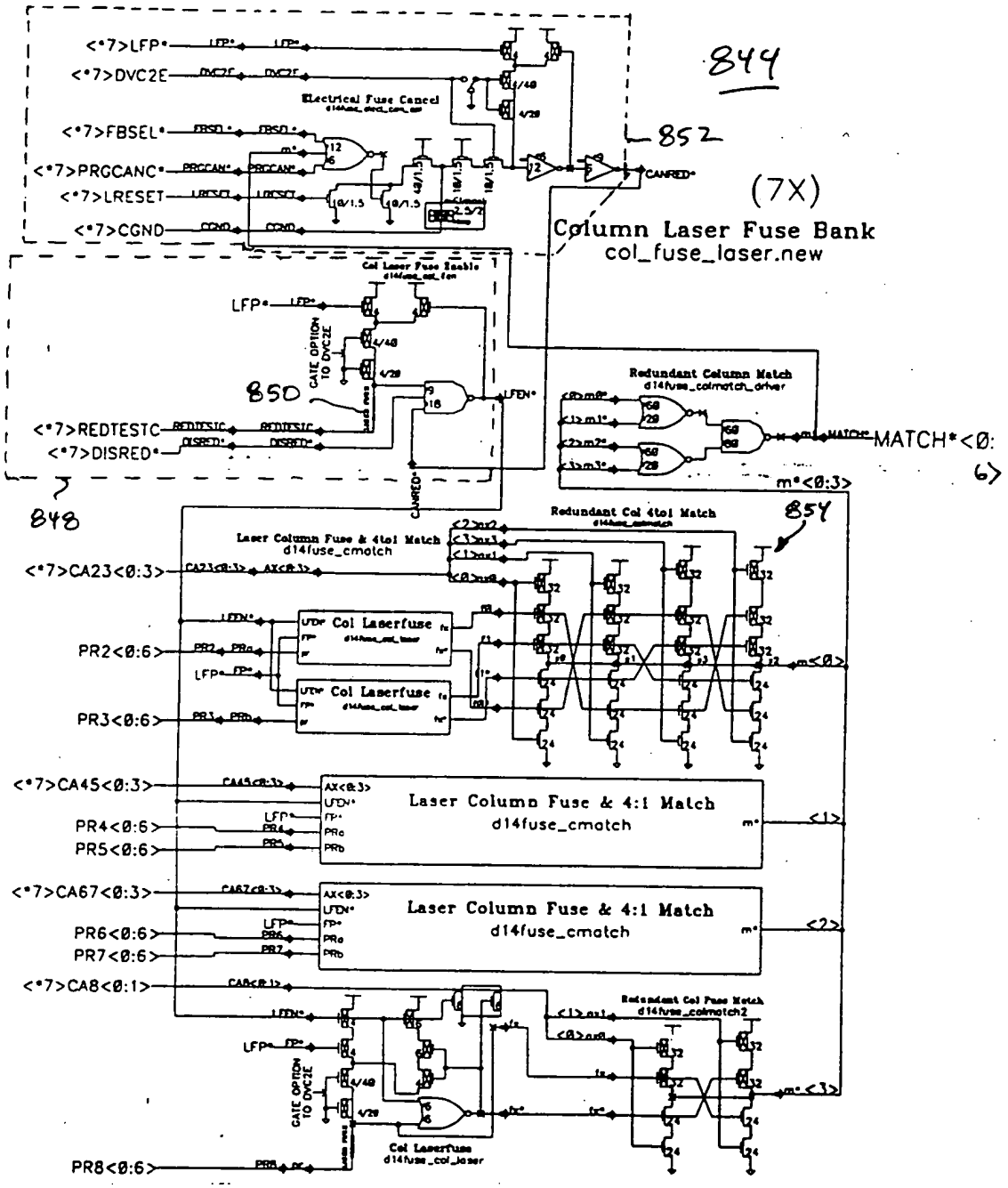


FIGURE 110

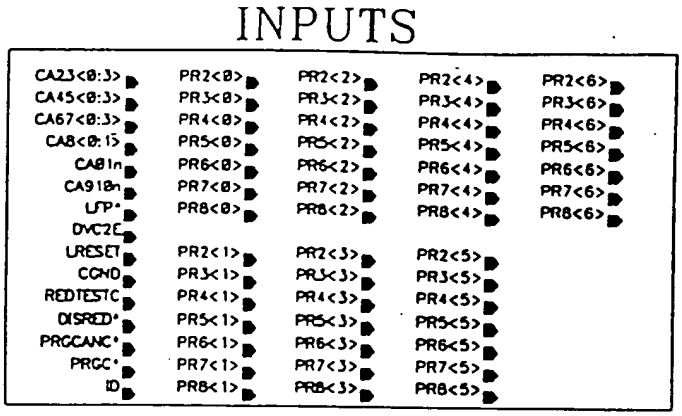

INPUTS
CA23<0:3>
CA45<0:3>
CA67<0:3>
CA8<0:1>
CA81n
CA918n
LFP*
DVC2E
LRESET
CGND
REDTESTC
DISRED*
PRGCANC*
PRGC*
ID
PR2<0>
PR3<0>
PR4<0>
PR5<0>
PR6<0>
PR7<0>
PR8<0>
PR2<1>
PR3<1>
PR4<1>
PR5<1>
PR6<1>
PR7<1>
PR8<1>
PR2<2>
PR3<2>
PR4<2>
PR5<2>
PR6<2>
PR7<2>
PR8<2>
PR2<3>
PR3<3>
PR4<3>
PR5<3>
PR6<3>
PR7<3>
PR8<3>
PR2<4>
PR3<4>
PR4<4>
PR5<4>
PR6<4>
PR7<4>
PR8<4>
PR2<5>
PR3<5>
PR4<5>
PR5<5>
PR6<5>
PR7<5>
PR8<5>
PR2<6>
PR3<6>
PR4<6>
PR5<6>
PR6<6>
PR7<6>
PR8<6>

FIGURE 111

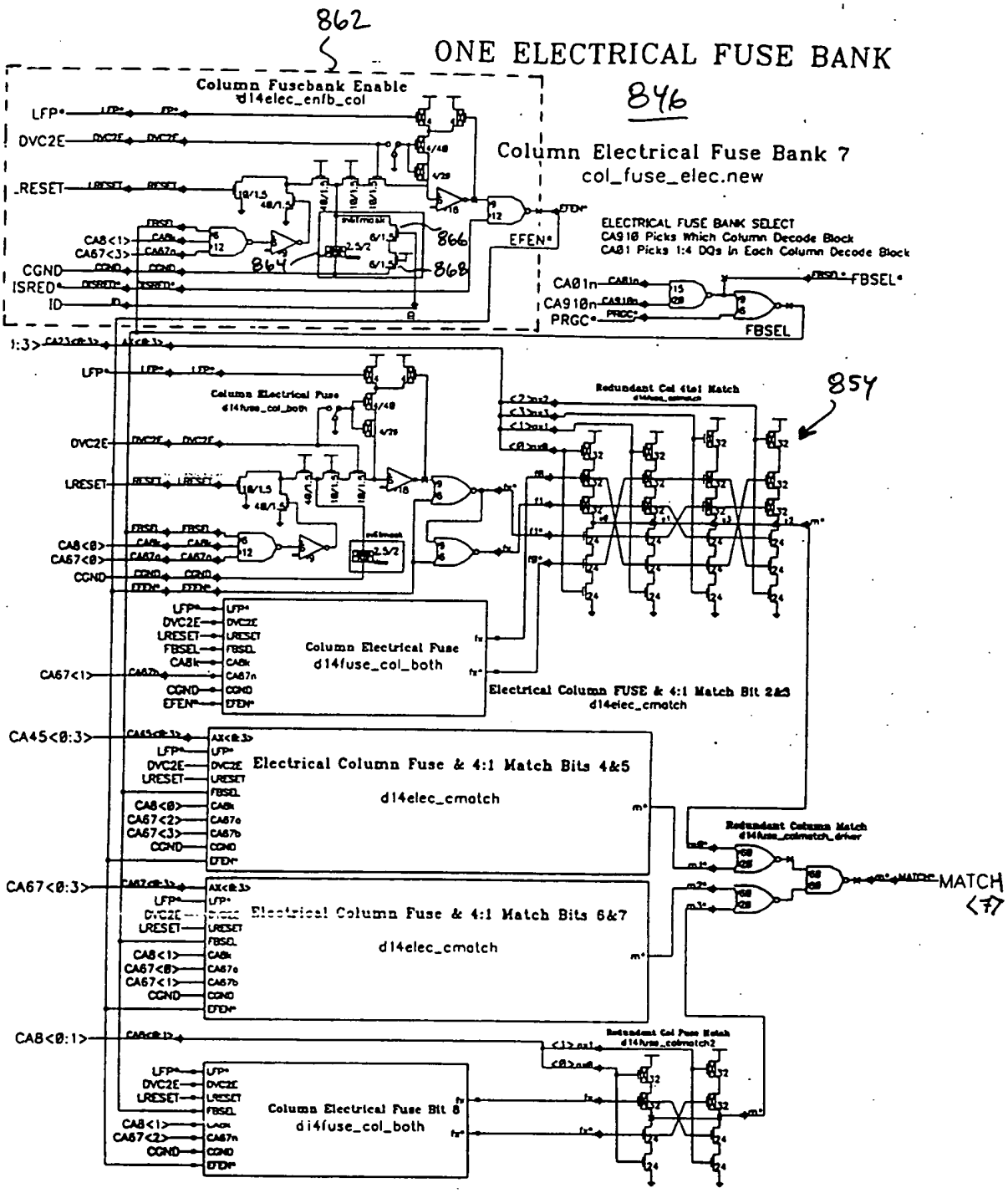

862
ONE ELECTRICAL FUSE BANK
846
Column Fusebank Enable
d14elec_enfb_col
Column Electrical Fuse Bank 7
col_fuse_elec.new
ELECTRICAL FUSE BANK SELECT
CA910 Picks Which Column Decode Block
CA01 Picks 1:4 DQs In Each Column Decode Block
LFP*
DVC2E
-RESET
CA8<1>
CA67<3>
CGND
ISRED*
ID
EFEN*
CA01n
CA910n
PRGC*
FBSEL*
FBSEL
866
864
868
854
Column Electrical Fuse
d14fuse_col_both
Redundant Col 4to1 Match
Electrical Column FUSE & 4:1 Match Bit 2&3
d14elec_cmatch
CA45<0:3>
Electrical Column Fuse & 4:1 Match Bits 4&5
d14elec_cmatch
CA67<0:3>
Electrical Column Fuse & 4:1 Match Bits 6&7
d14elec_cmatch
Redundant Column Match
MATCH
<7>
CA8<0:1>
Column Electrical Fuse Bit 8
d14fuse_col_both

FIGURE 112

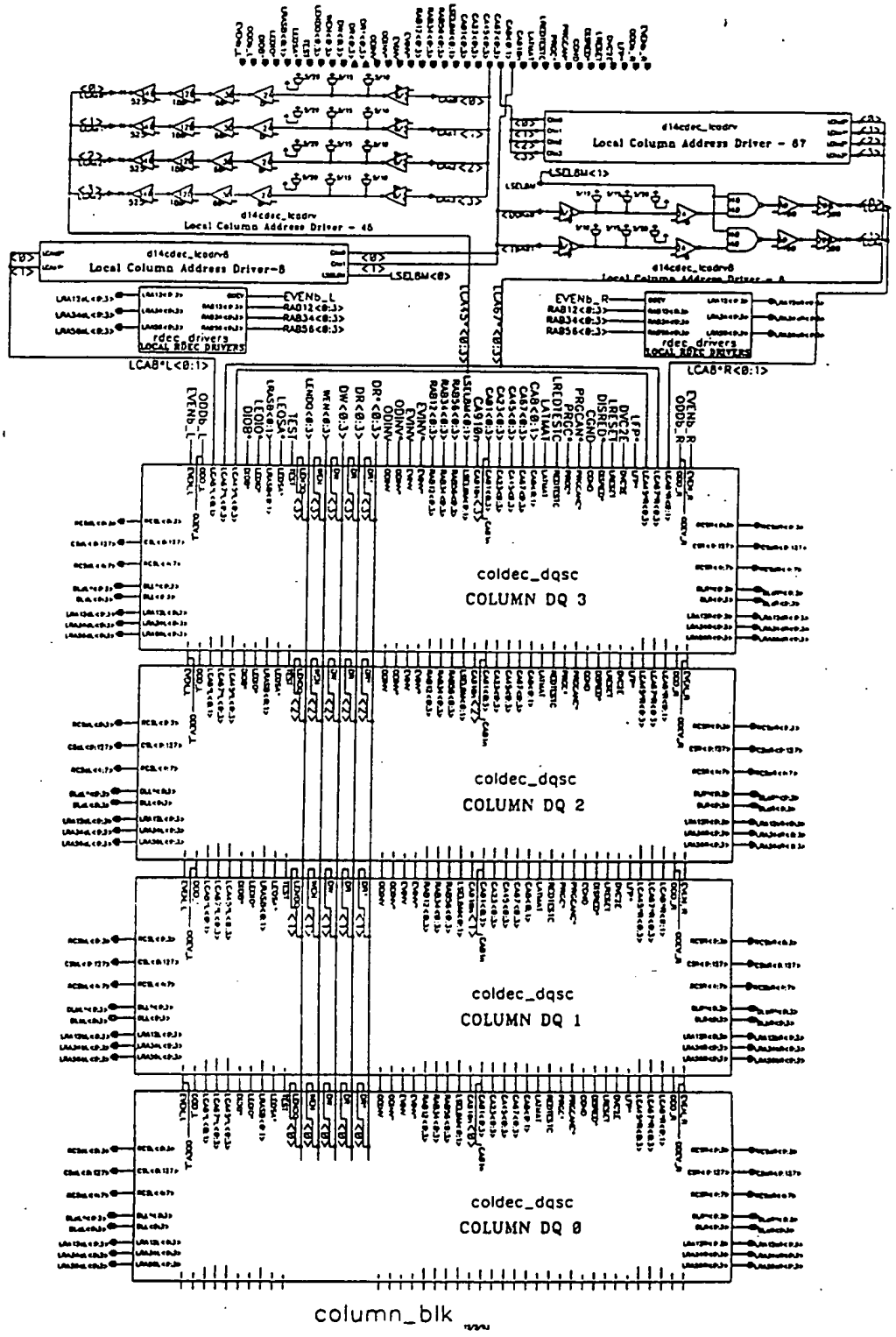

d14cdec_kcdrv
Local Column Address Driver - 67
d14cdec_kcdrv
Local Column Address Driver - 45
d14cdec_kcdrv8
Local Column Address Driver-8
d14cdec_kcdrv8
EVENb_L
RAB12<0:3>
RAB34<0:3>
RAB56<0:3>
rdec drivers
LOCAL RDEC DRIVERS
LCAB*L<0:1>
EVENb_R
LCAB*R<0:1>
coldec_dqsc
COLUMN DQ 3
coldec_dqsc
COLUMN DQ 2
coldec_dqsc
COLUMN DQ 1
coldec_dqsc
COLUMN DQ 0
column_blk

FIGURE 113

INPUTS FROM PERIPH.

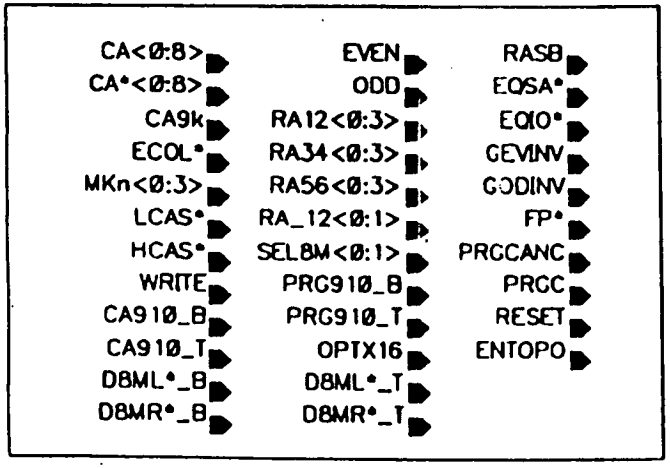


FIGURE 114

OUTPUTS TO COLUMN BLOCK

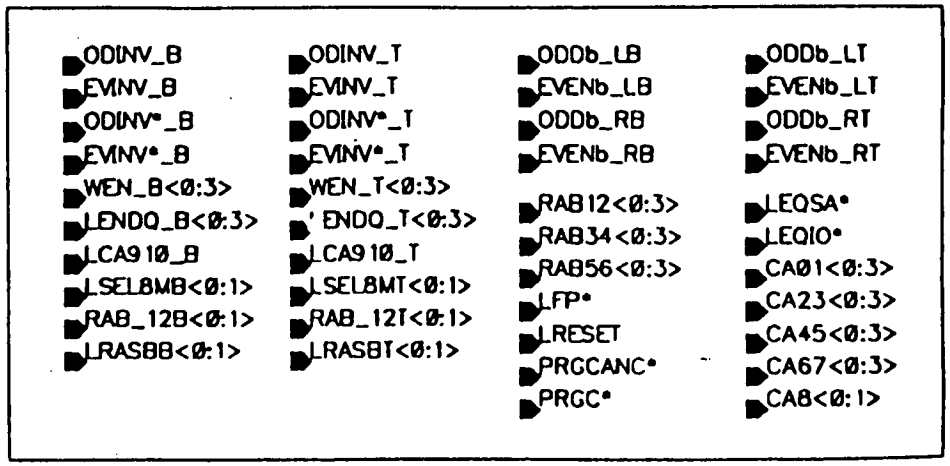


FIGURE 115

SIGNALS PASSING THROUGH

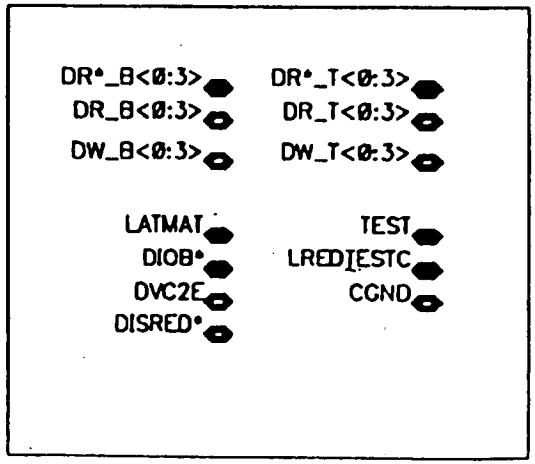


FIGURE 116

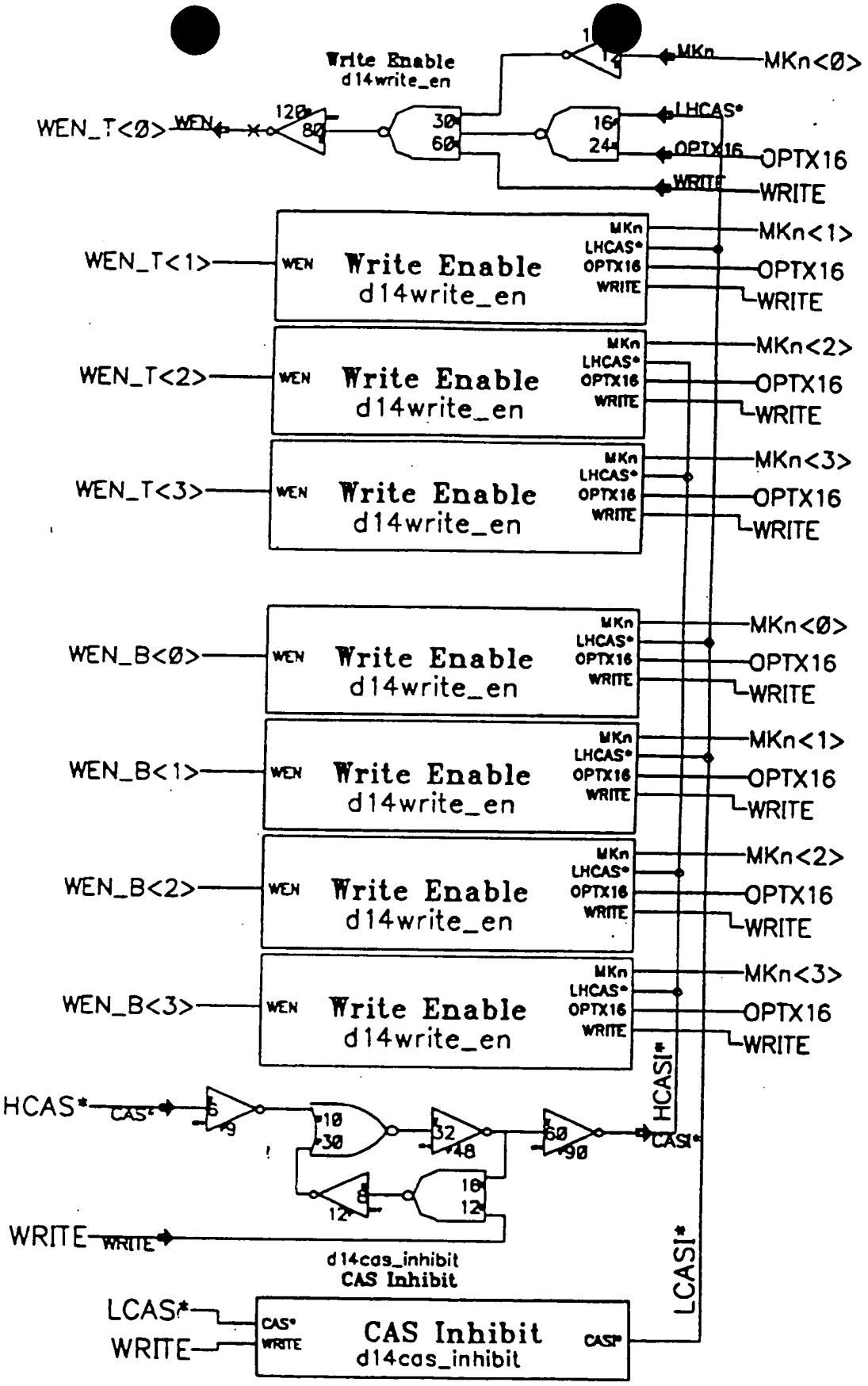

Write Enable
d14write_en
WEN_T<0>
WEN
MKn
MKn<0>
LHCAS*
OPTX16
WRITE
WEN_T<1>
WEN_T<2>
WEN_T<3>
MKn<1>
MKn<2>
MKn<3>
WEN_B<0>
WEN_B<1>
WEN_B<2>
WEN_B<3>
HCAS*
CAS*
HCASI*
CASI*
WRITE
d14cas_inhibit
CAS Inhibit
LCAS*
LCASI*

FIGURE 117

INPUTS FROM BOTTOM ROW RED.

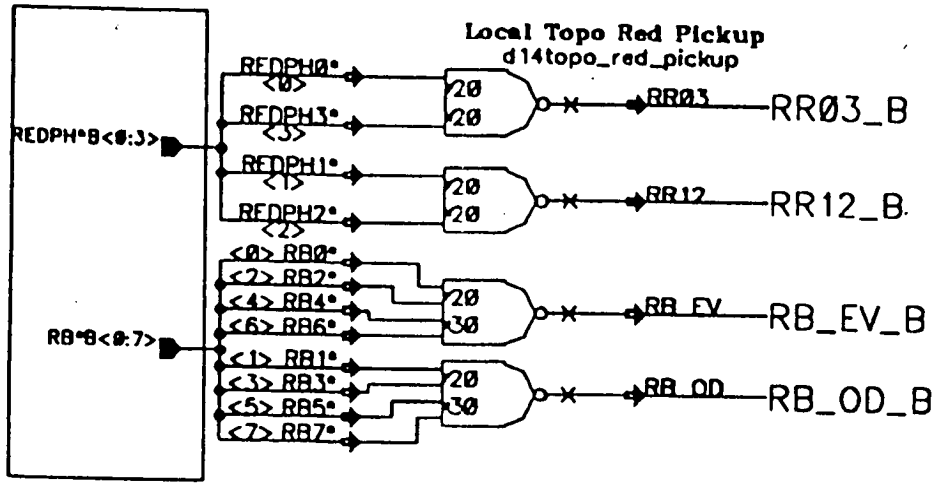


FIGURE 118

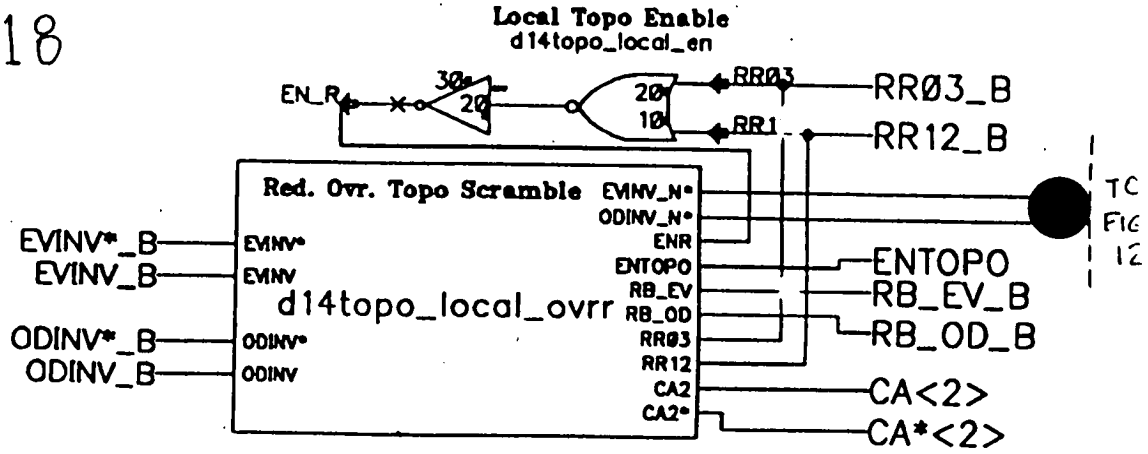


FIGURE 119

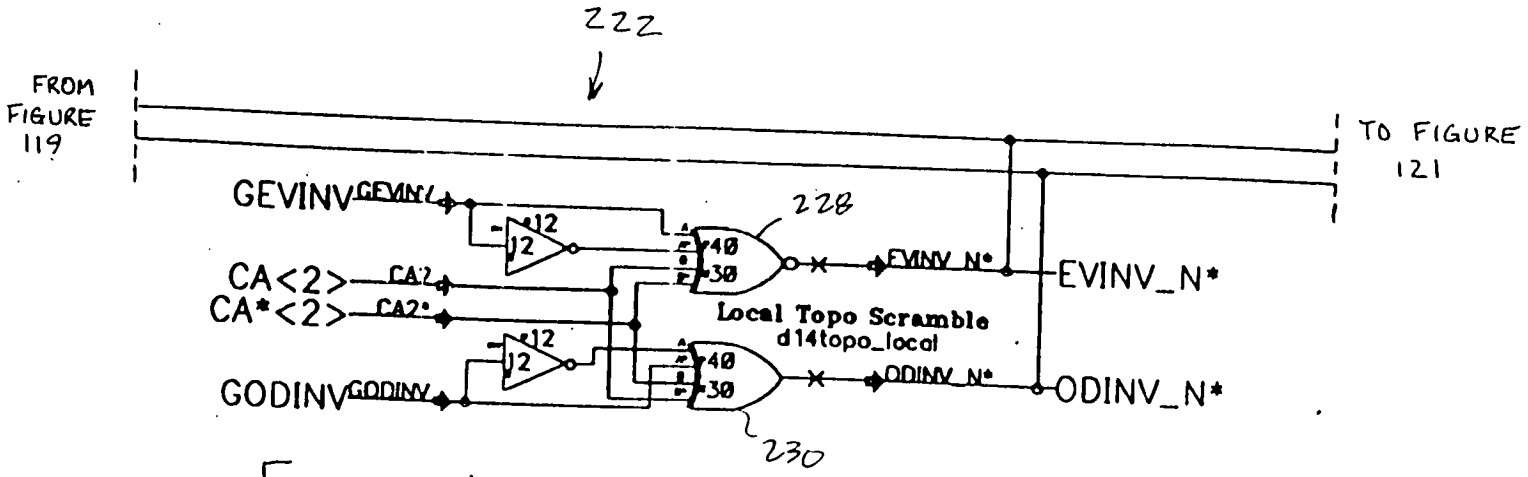


FIGURE 120

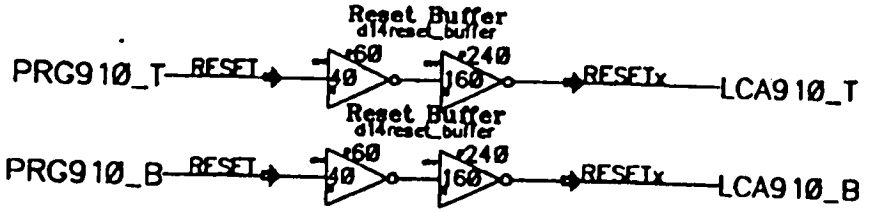


FIGURE 122

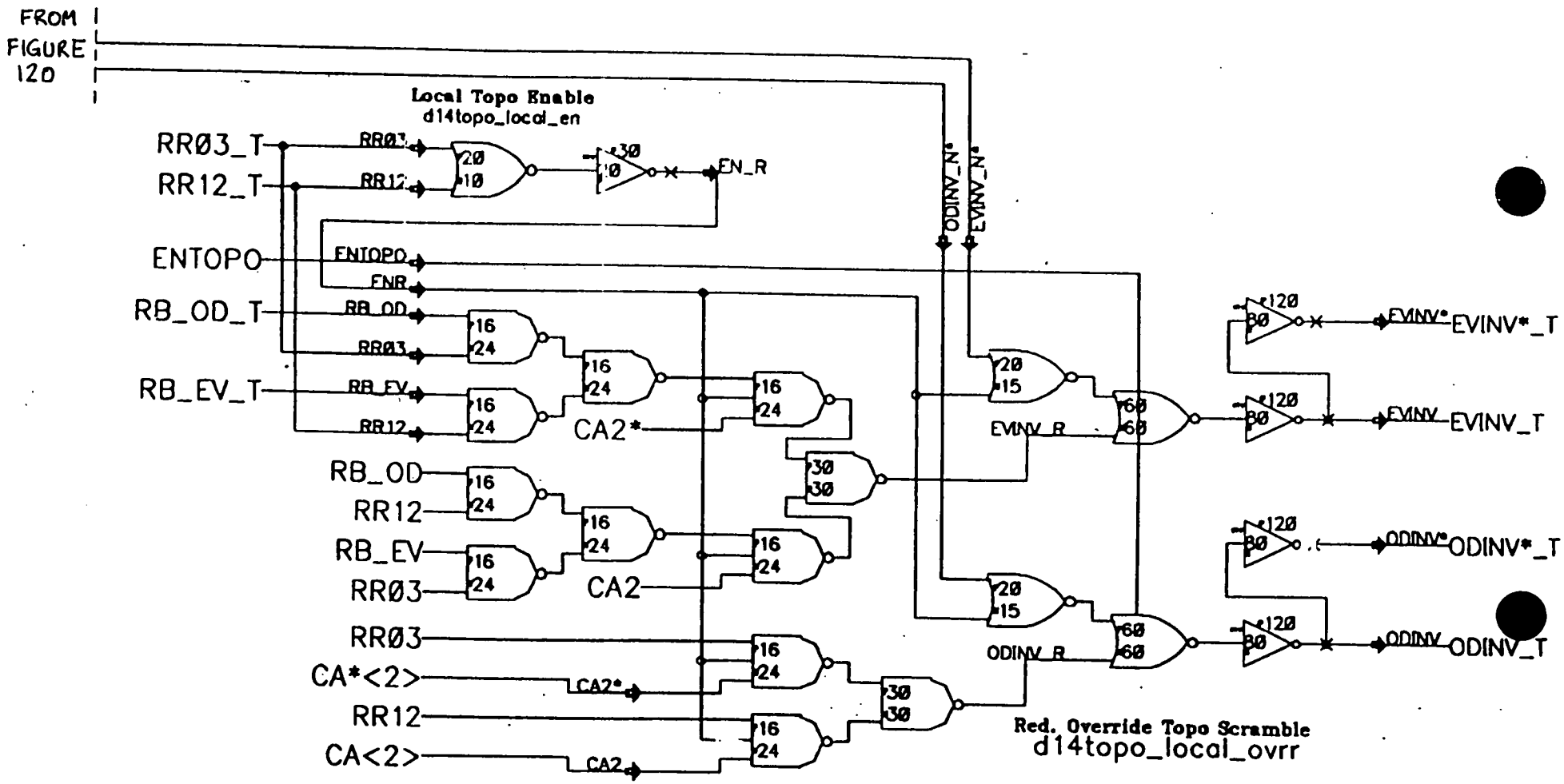

FROM FIGURE 120
Local Topo Enable
d14topo_local_en
RR03_T
RR12_T
ENTOPO
RB_OD_T
RB_EV_T
EN_R
ENTOPO
ENR
RB_OD
RR03
RB_EV
RR12
CA2*
RB_OD
RR12
RB_EV
RR03
CA2
RR03
CA*<2>
CA2*
RR12
CA<2>
CA2
ODINV_N*
EVINV_N*
EVINV_R
ODINV_R
EVINV*
EVINV*_T
EVINV
EVINV_T
ODINV*
ODINV*_T
ODINV
ODINV_T
Red. Override Topo Scramble
d14topo_local_ovrr

FIGURE 121

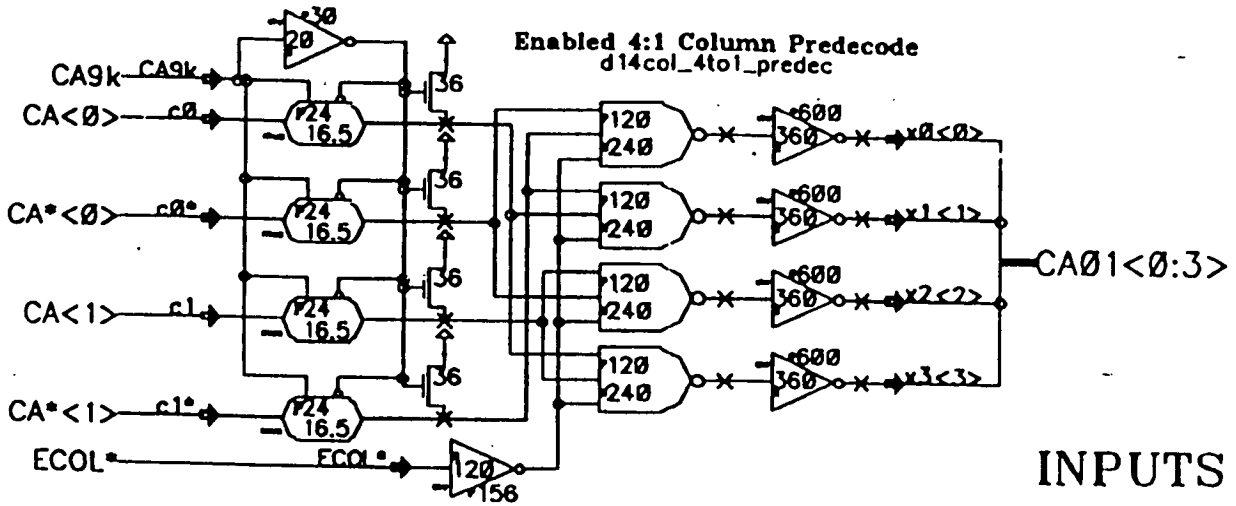


FIGURE 123

INPUTS FROM TOP ROW RED.

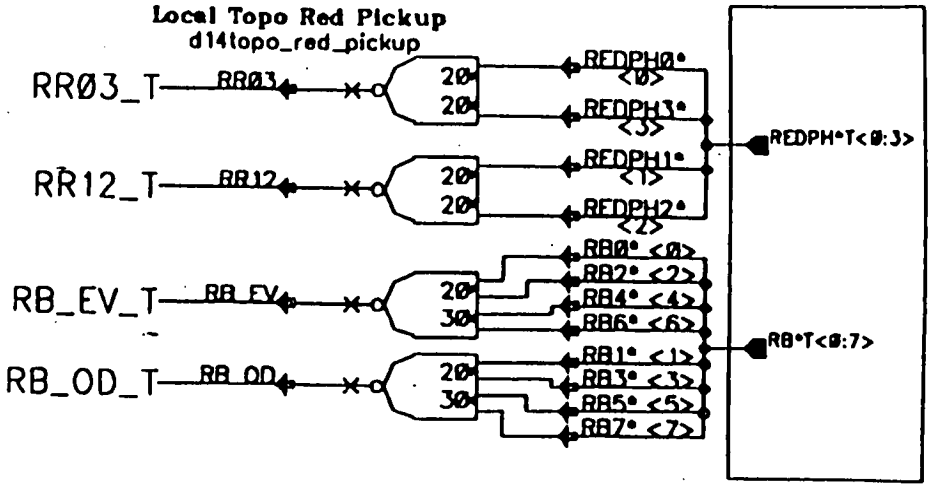


FIGURE 124

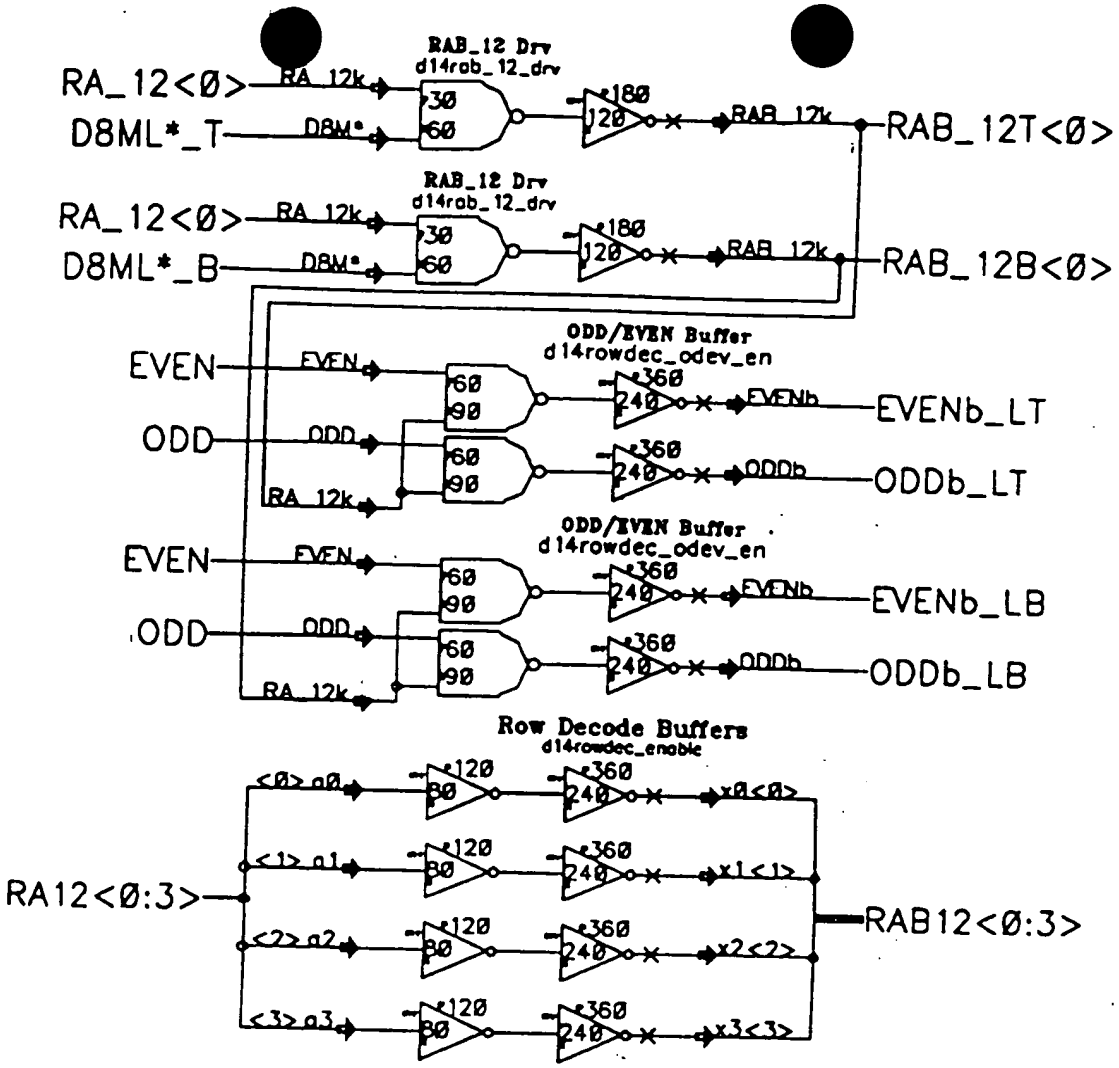


FIGURE 125

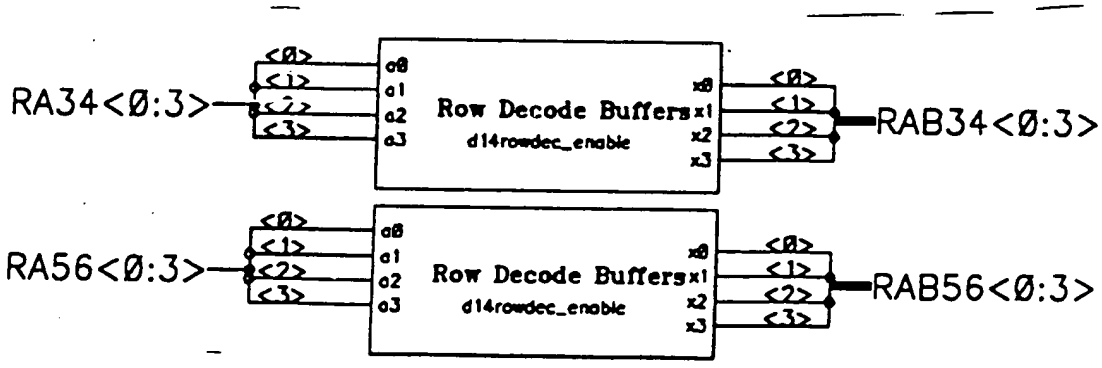


FIGURE 126

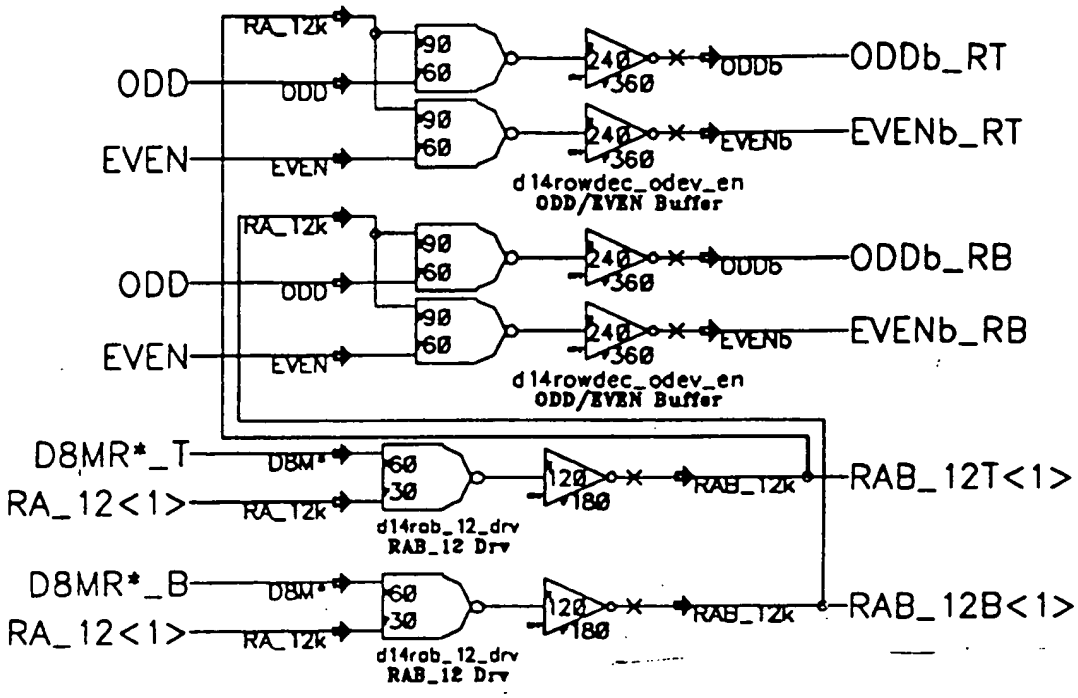

RA_12k
ODD
EVEN
90
60
240
360
ODDb
EVENb
ODDb_RT
EVENb_RT
d14rowdec_odev_en
ODD/EVEN Buffer
ODDb_RB
EVENb_RB
D8MR*_T
D8MR*_B
RA_12<1>
60
30
120
180
RAB_12k
d14rab_12_drv
RAB_12 Drv
RAB_12T<1>
RAB_12B<1>

FIGURE 127

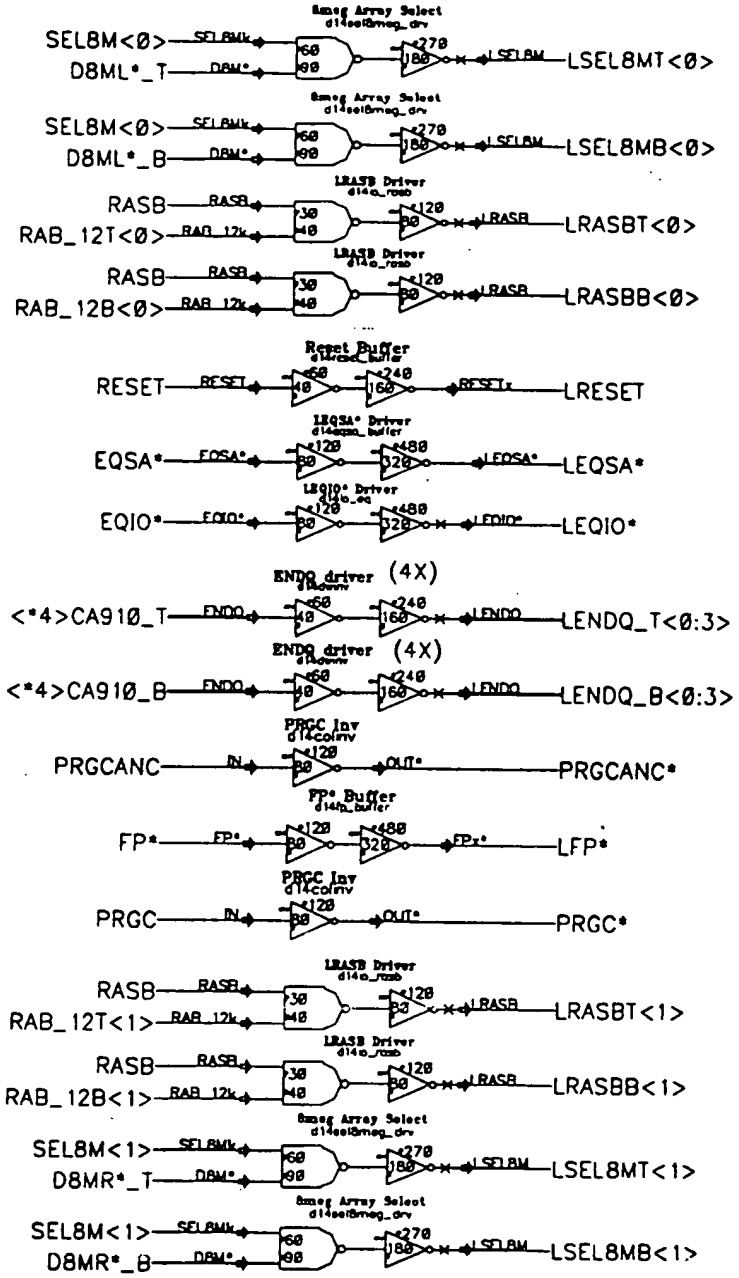

8meg Array Select
SEL8M<0>
D8ML*_T
LSEL8MT<0>
SEL8M<0>
D8ML*_B
LSEL8MB<0>
LRASB Driver
RASB
RAB_12T<0>
LRASBT<0>
RASB
RAB_12B<0>
LRASBB<0>
Reset Buffer
RESET
LRESET
LEQSA* Driver
EQSA*
LEQSA*
LEQIO* Driver
EQIO*
LEQIO*
ENDQ driver (4X)
<*4>CA910_T
LENDQ_T<0:3>
ENDQ driver (4X)
<*4>CA910_B
LENDQ_B<0:3>
PRGC Inv
PRGCANC
PRGCANC*
FP* Buffer
FP*
LFP*
PRGC Inv
PRGC
PRGC*
LRASB Driver
RASB
RAB_12T<1>
LRASBT<1>
LRASB Driver
RASB
RAB_12B<1>
LRASBB<1>
8meg Array Select
SEL8M<1>
D8MR*_T
LSEL8MT<1>
8meg Array Select
SEL8M<1>
D8MR*_B
LSEL8MB<1>

FIGURE 128

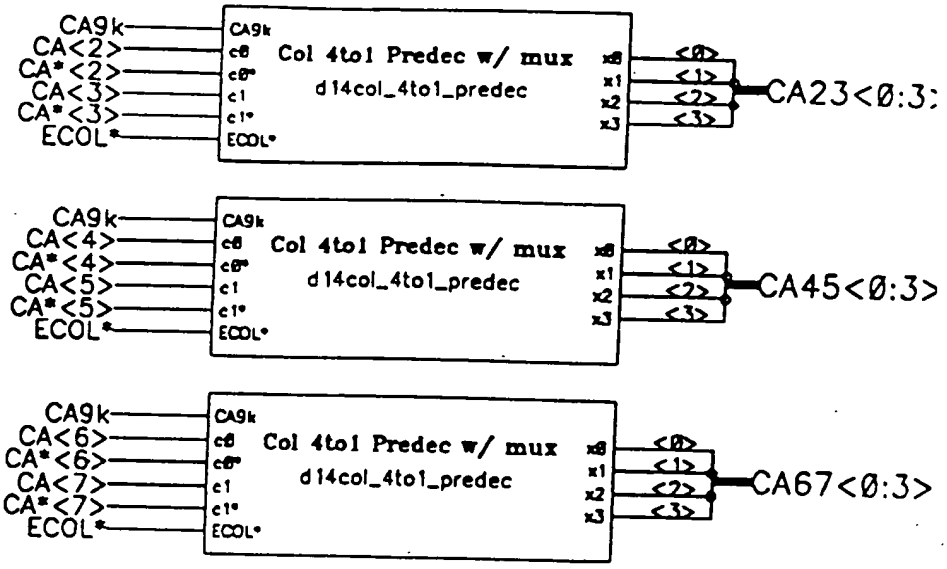


FIGURE 129

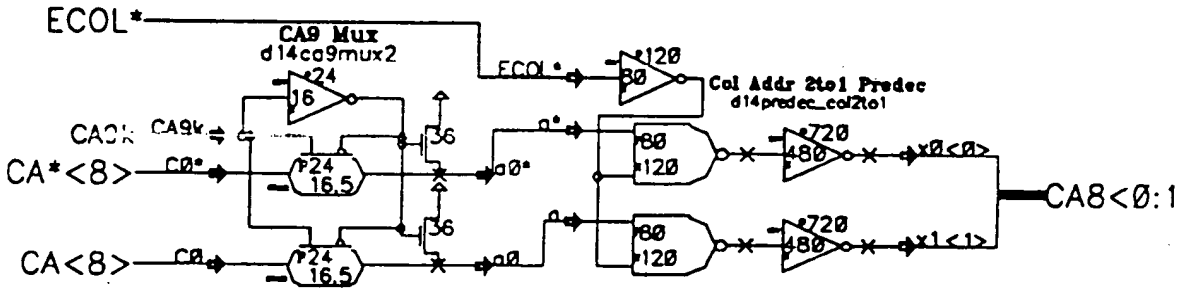


FIGURE 130

INPUTS

OUTPUTS

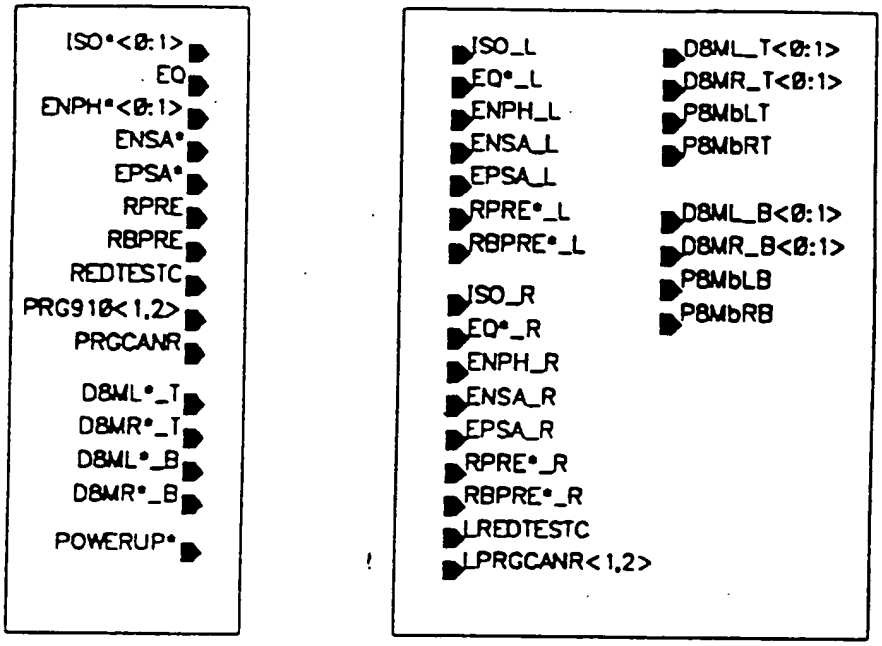


FIGURE 131

RIGHTSIDE OF PERIPH GAP

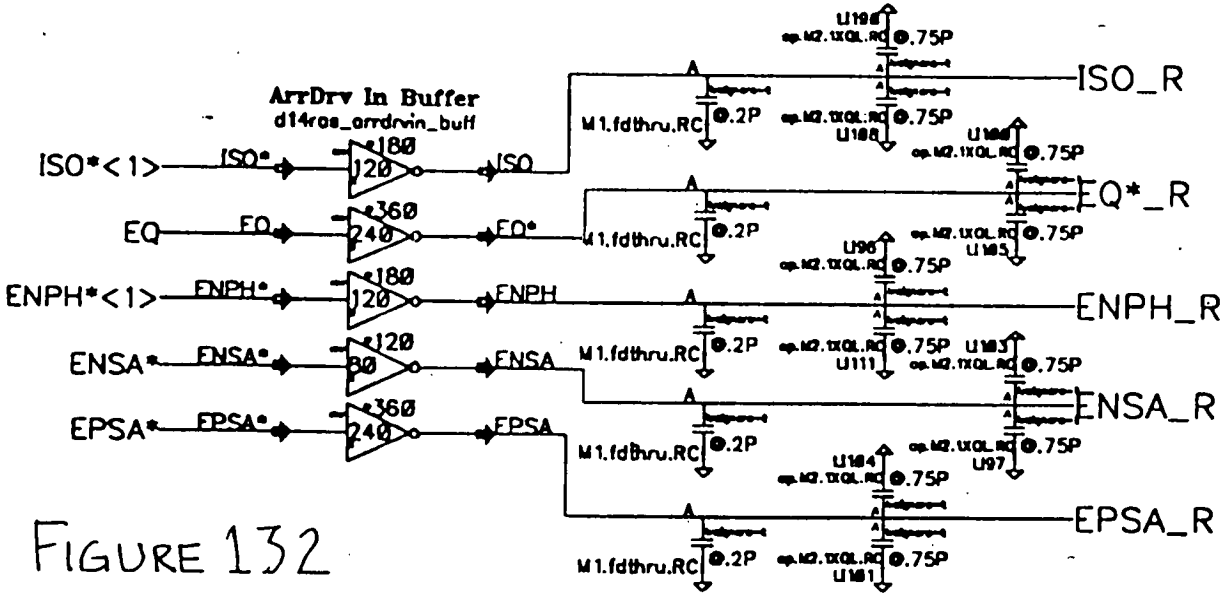


FIGURE 132

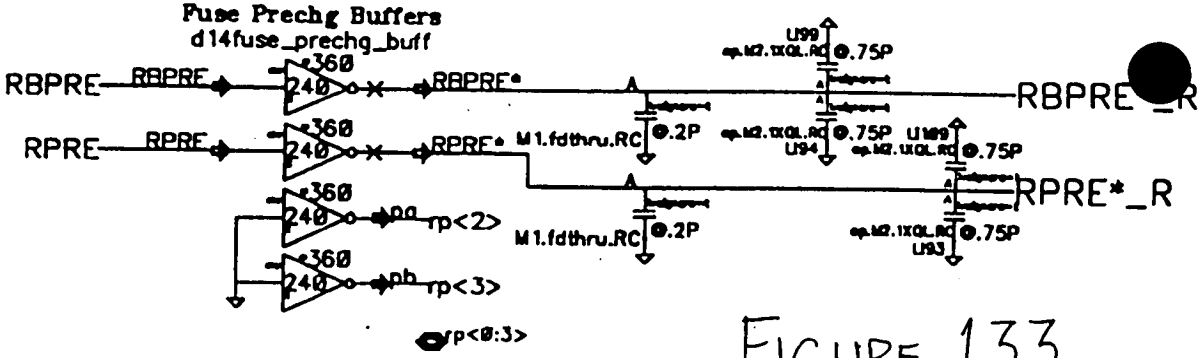


FIGURE 133

LEFTSIDE OF PERIPH GAP

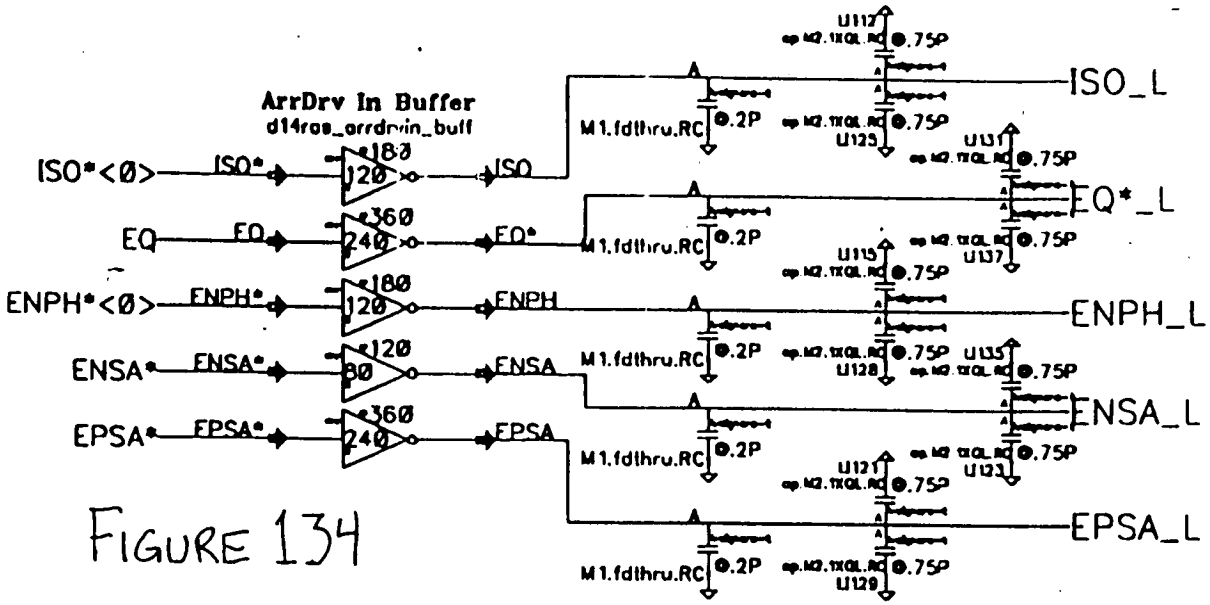


FIGURE 134

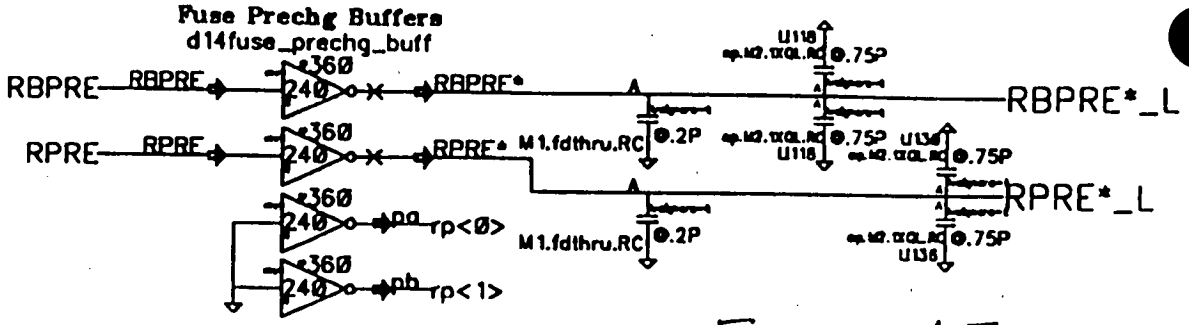


FIGURE 135

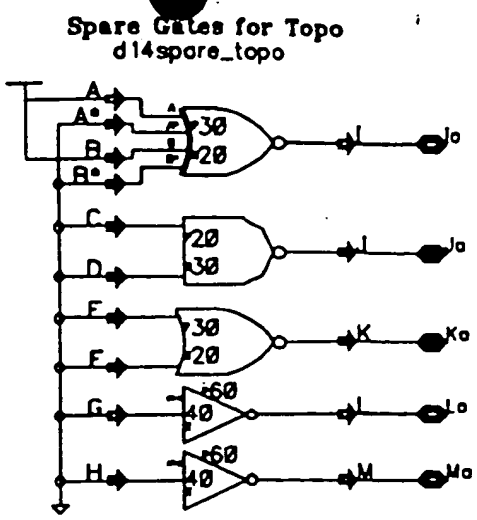


FIGURE 136

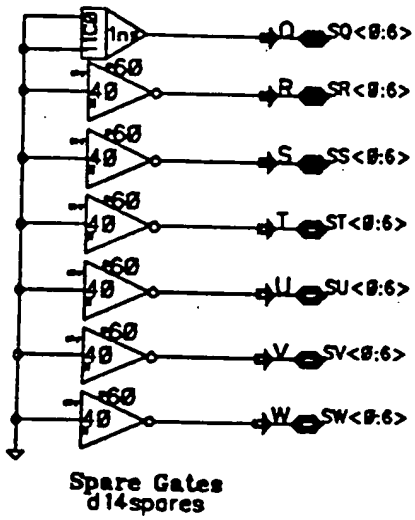


FIGURE 137

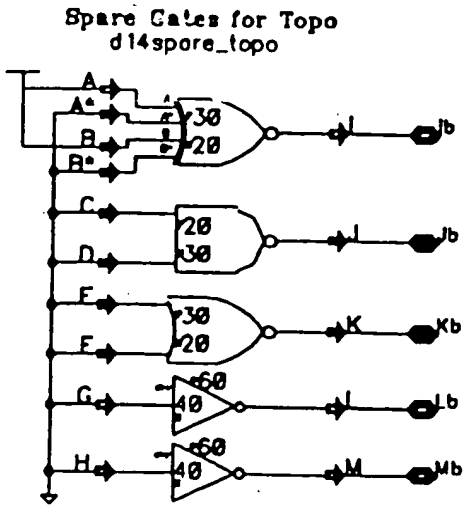


FIGURE 138

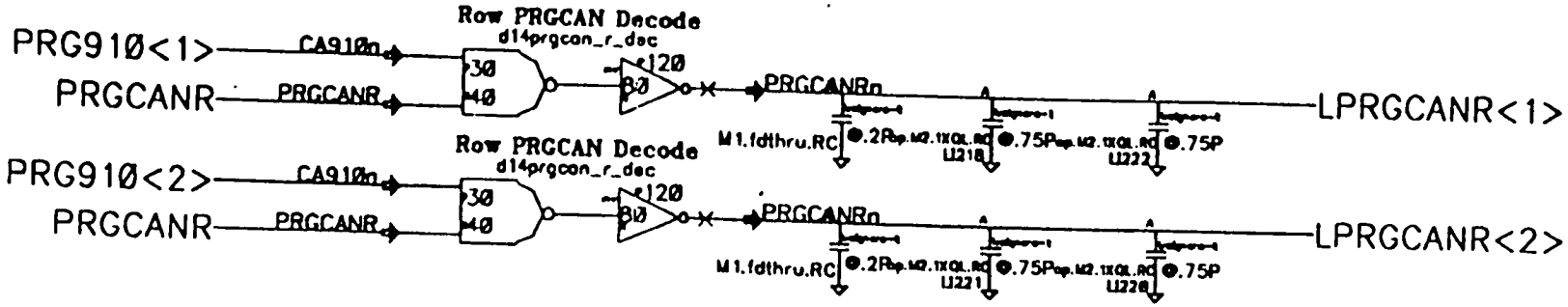

PRG910<1>
CA910n
PRGCANR
PRGCANR
Row PRGCAN Decode
d14prgcon_r_dec
30
40
120
80
PRGCANRn
M1.fdthru.RC
.2P
.75P
.75P
LPRGCANR<1>
PRG910<2>
CA910n
PRGCANR
PRGCANR
Row PRGCAN Decode
d14prgcon_r_dec
30
40
120
80
PRGCANRn
M1.fdthru.RC
.2P
.75P
.75P
LPRGCANR<2>

FIGURE 139

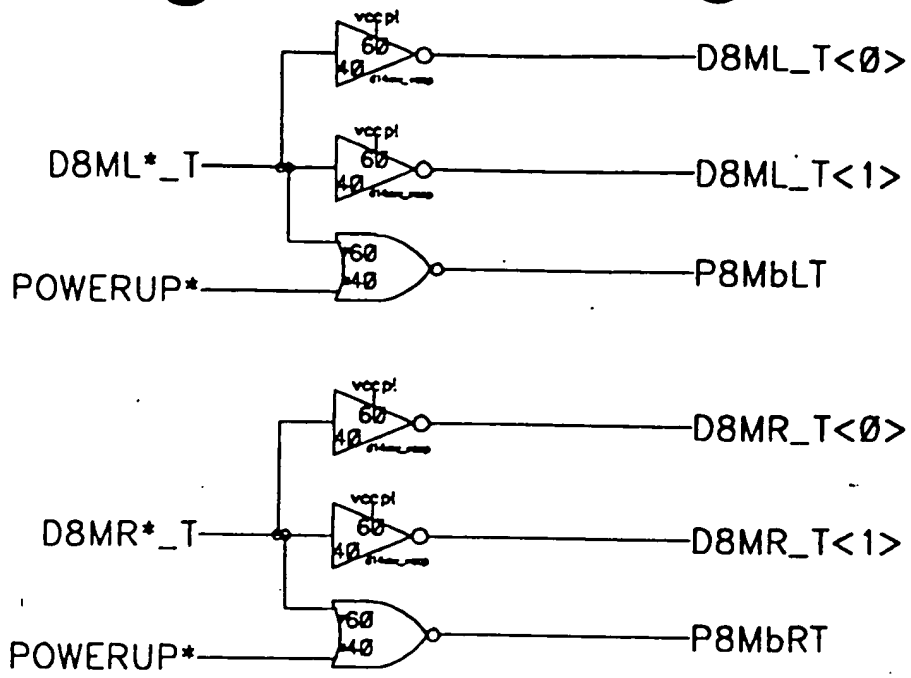


FIGURE 140

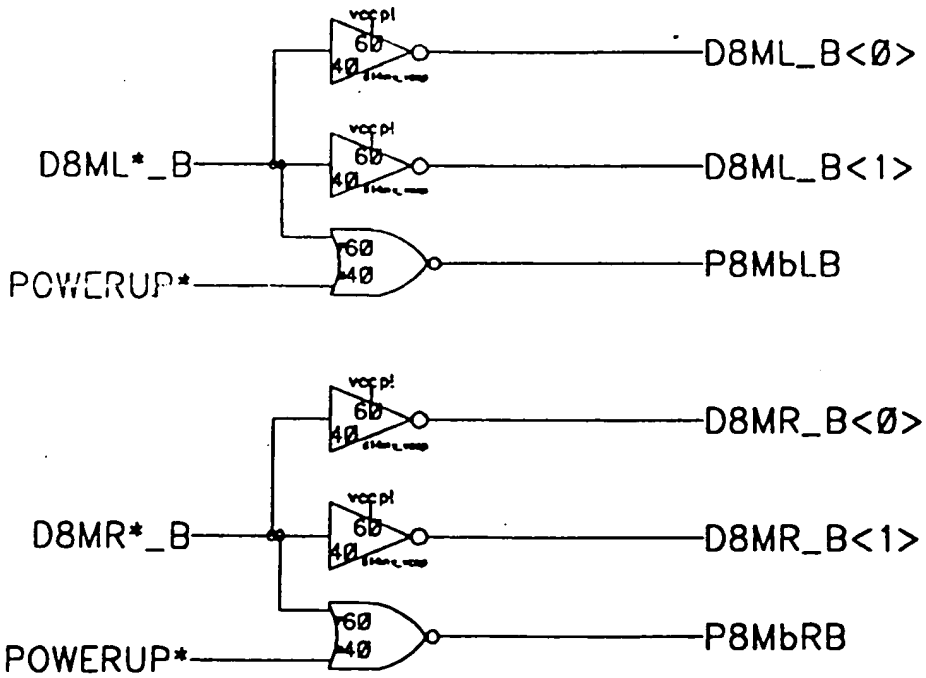


FIGURE 141

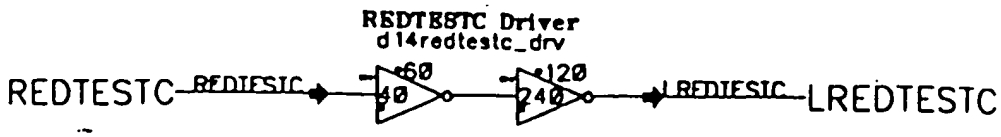

REDTESTC Driver
d14redtestc_drv
REDTESTC
REDTESTC
60
30
120
240
LREDTESTC
LREDTESTC

FIGURE 142

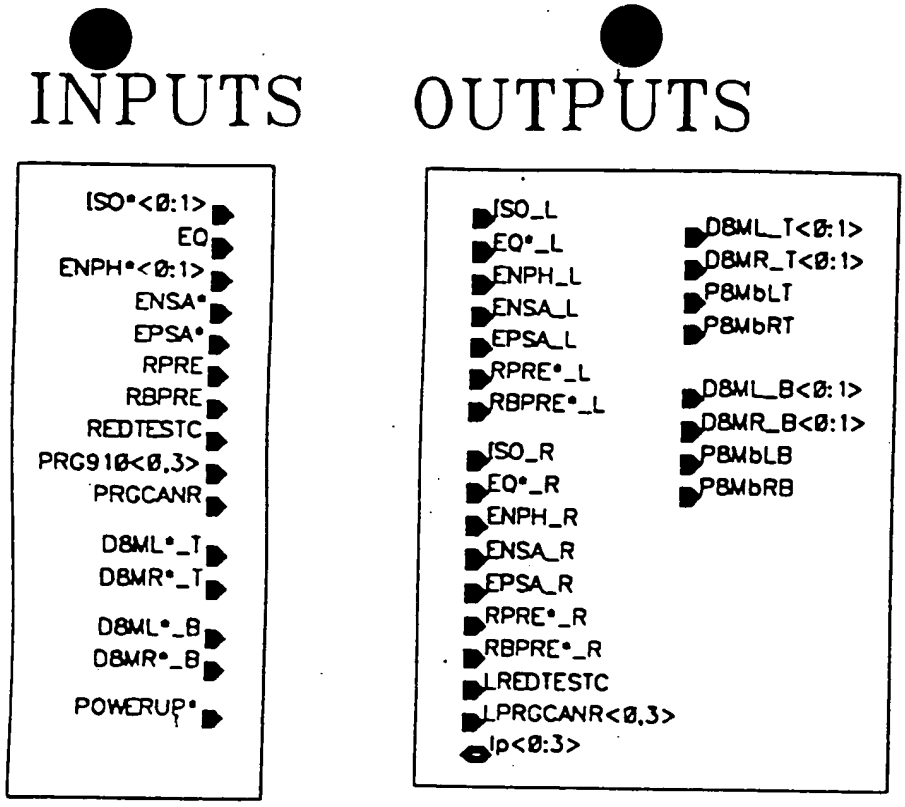

INPUTS
OUTPUTS
ISO*<0:1>
EQ
ENPH*<0:1>
ENSA*
EPSA*
RPRE
RBPRE
REDTESTC
PRG910<0,3>
PRGCANR
D8ML*_T
D8MR*_T
D8ML*_B
D8MR*_B
POWERUP*
ISO_L
EQ*_L
ENPH_L
ENSA_L
EPSA_L
RPRE*_L
RBPRE*_L
ISO_R
EQ*_R
ENPH_R
ENSA_R
EPSA_R
RPRE*_R
RBPRE*_R
LREDTESTC
LPRGCANR<0,3>
lp<0:3>
D8ML_T<0:1>
D8MR_T<0:1>
P8MbLT
P8MbRT
D8ML_B<0:1>
D8MR_B<0:1>
P8MbLB
P8MbRB

FIGURE 143

LEFTSIDE OF PERIPH GAP

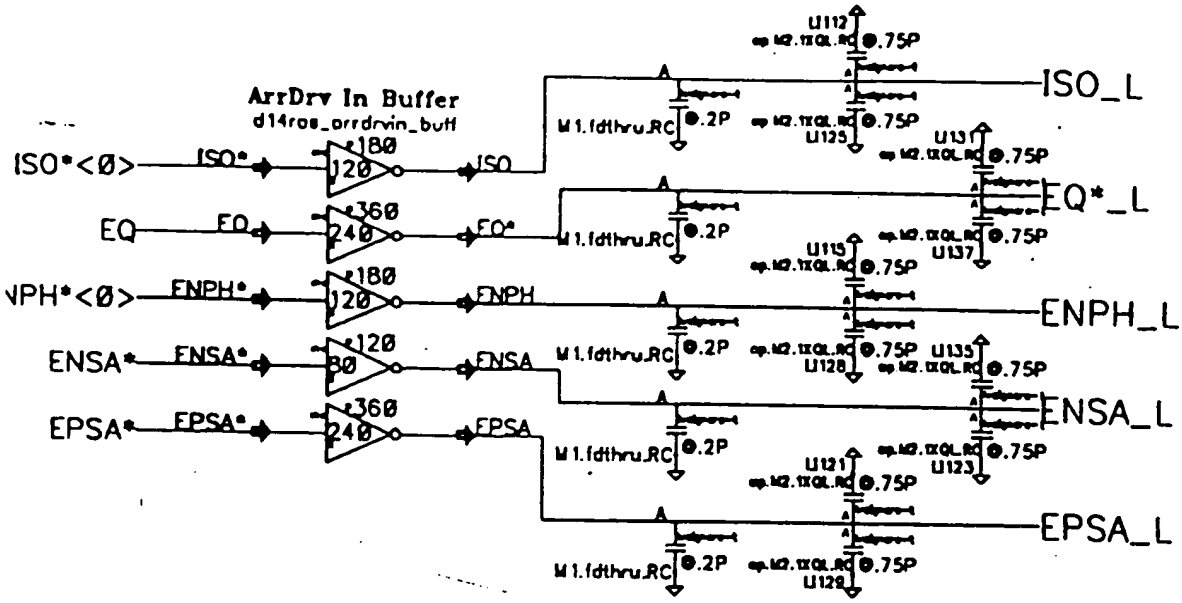


FIGURE 144

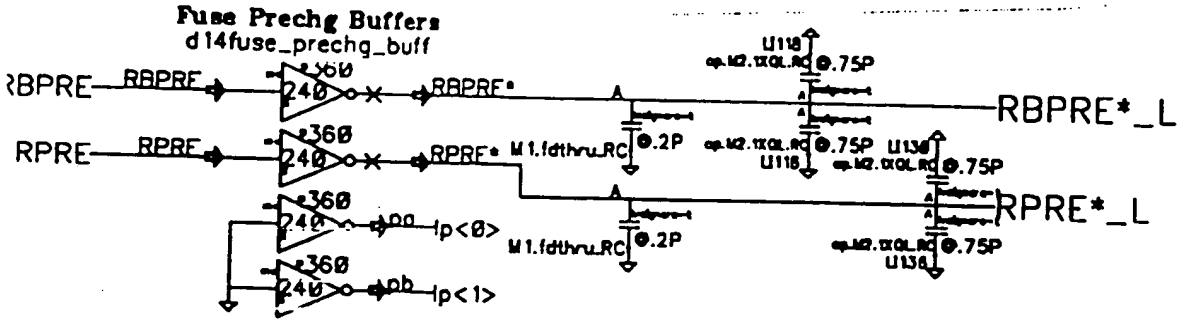


FIGURE 145

RIGHTSIDE OF PERIPH GAP

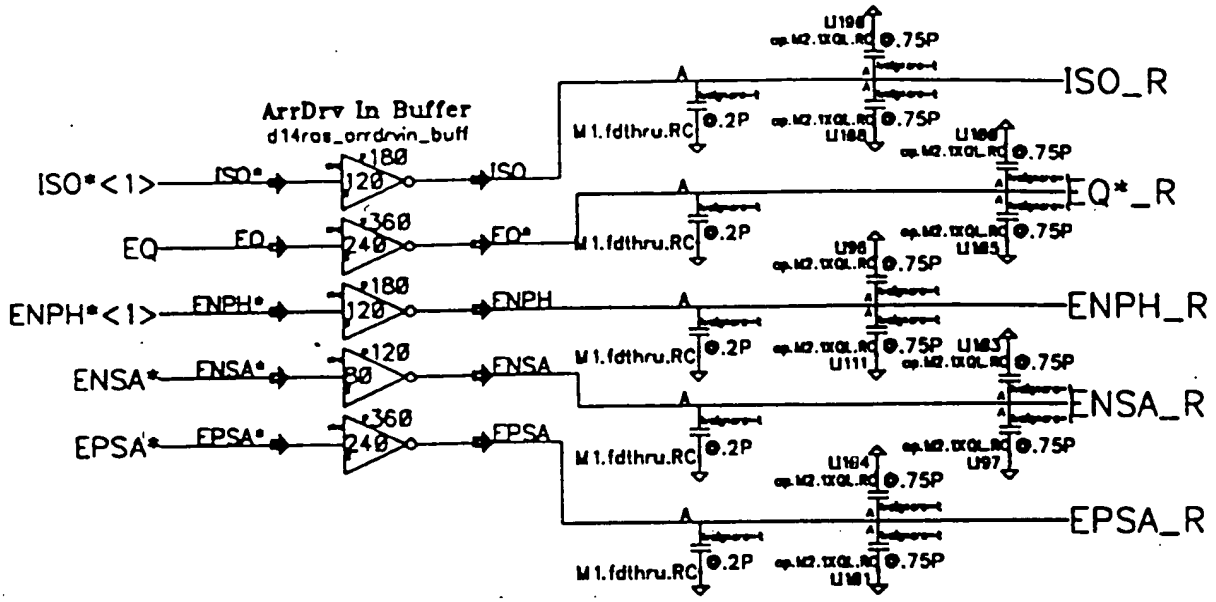


FIGURE 146

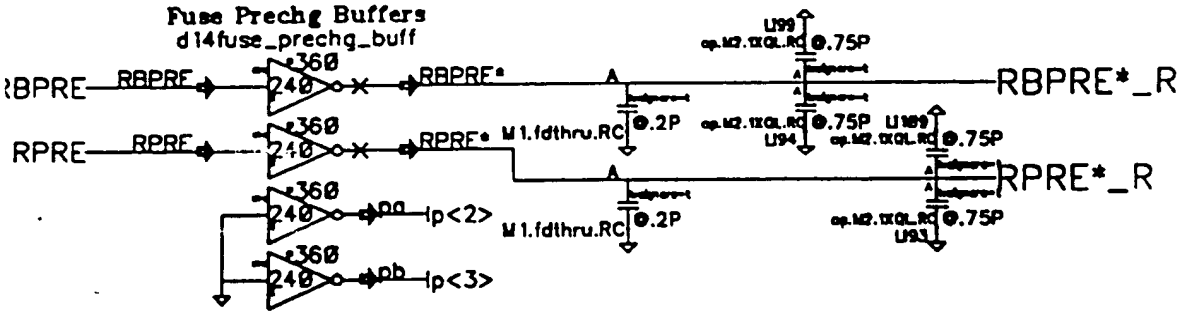


FIGURE 147

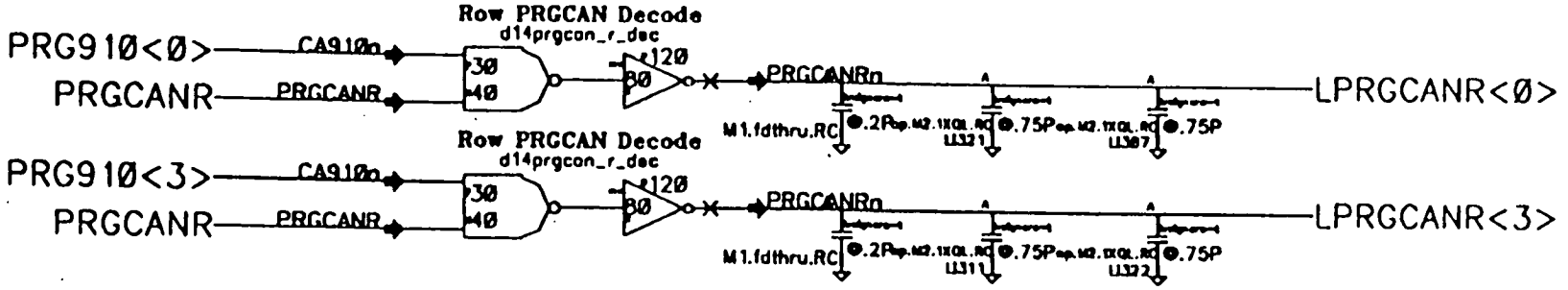


FIGURE 148

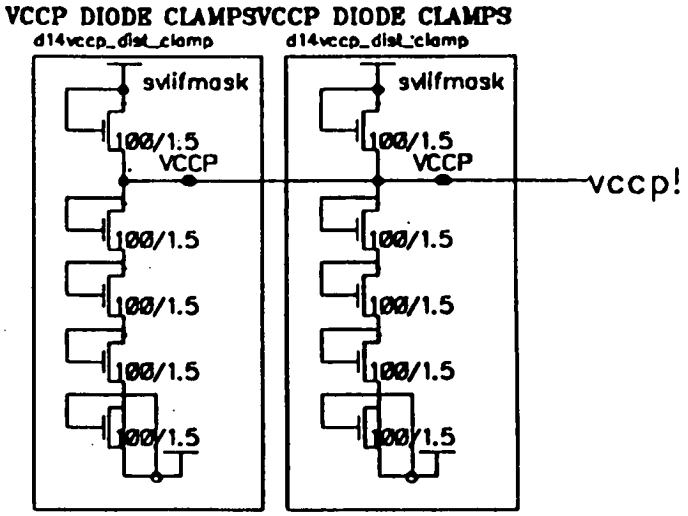


FIGURE 149

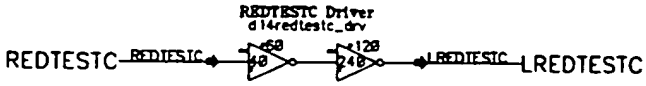


FIGURE 150

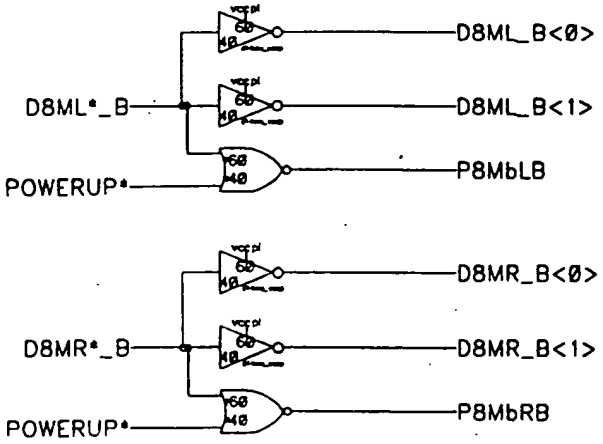


FIGURE 151

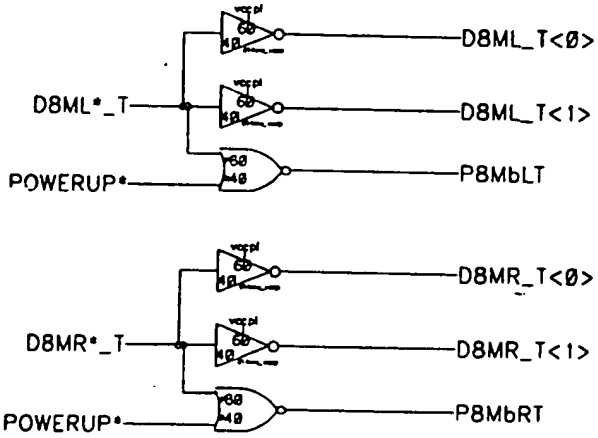


FIGURE 152

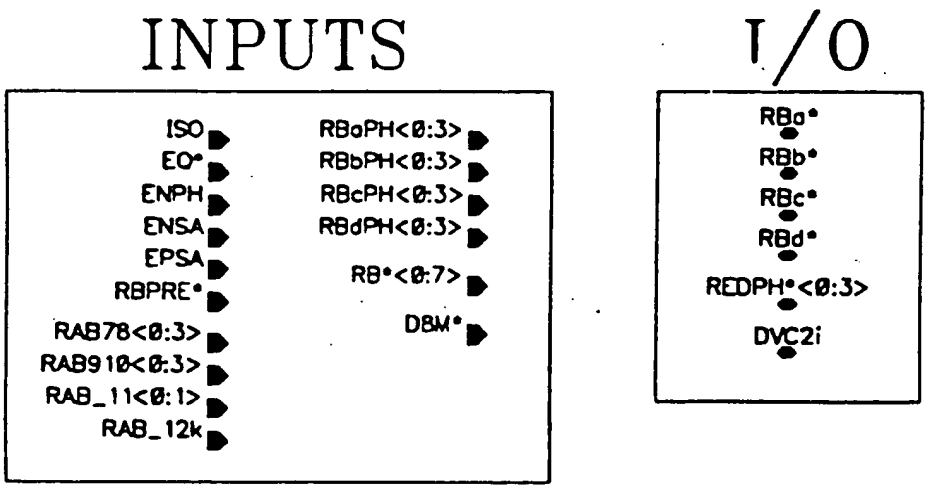

INPUTS
I/O
ISO
EO*
ENPH
ENSA
EPSA
RBPRE*
RAB78<0:3>
RAB910<0:3>
RAB_11<0:1>
RAB_12k
RBaPH<0:3>
RBbPH<0:3>
RBcPH<0:3>
RBdPH<0:3>
RB*<0:7>
DBM*
RBa*
RBb*
RBc*
RBd*
REDPH*<0:3>
DVC2i

FIGURE 153

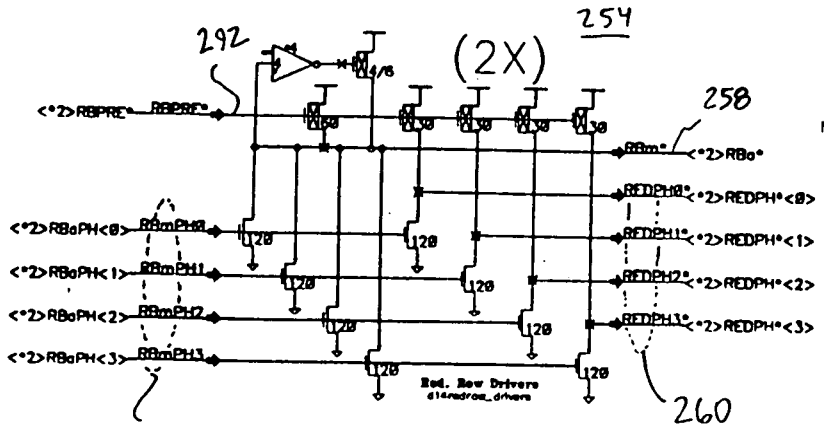


FIGURE 154

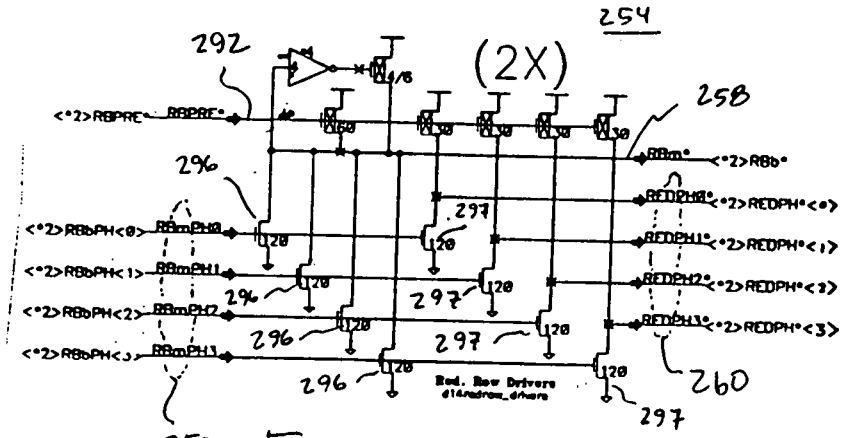


FIGURE 155

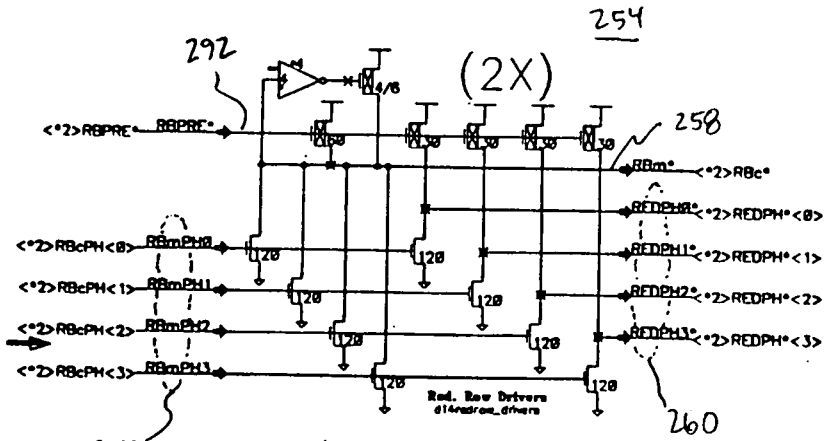


FIGURE 156

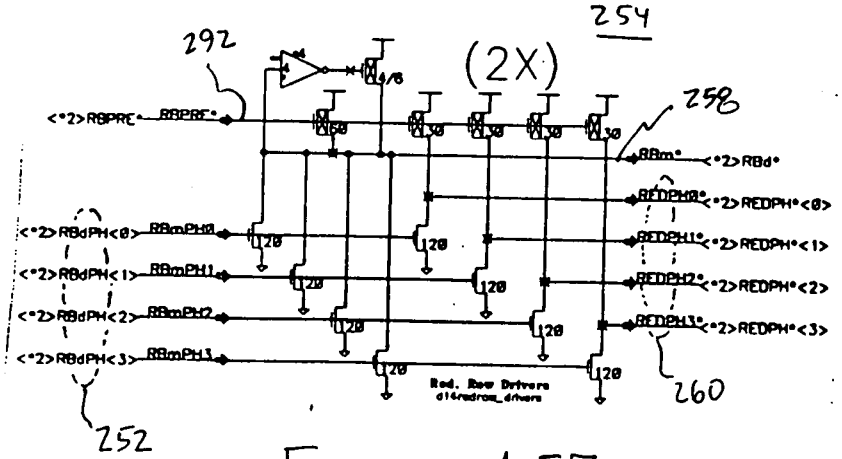


FIGURE 157

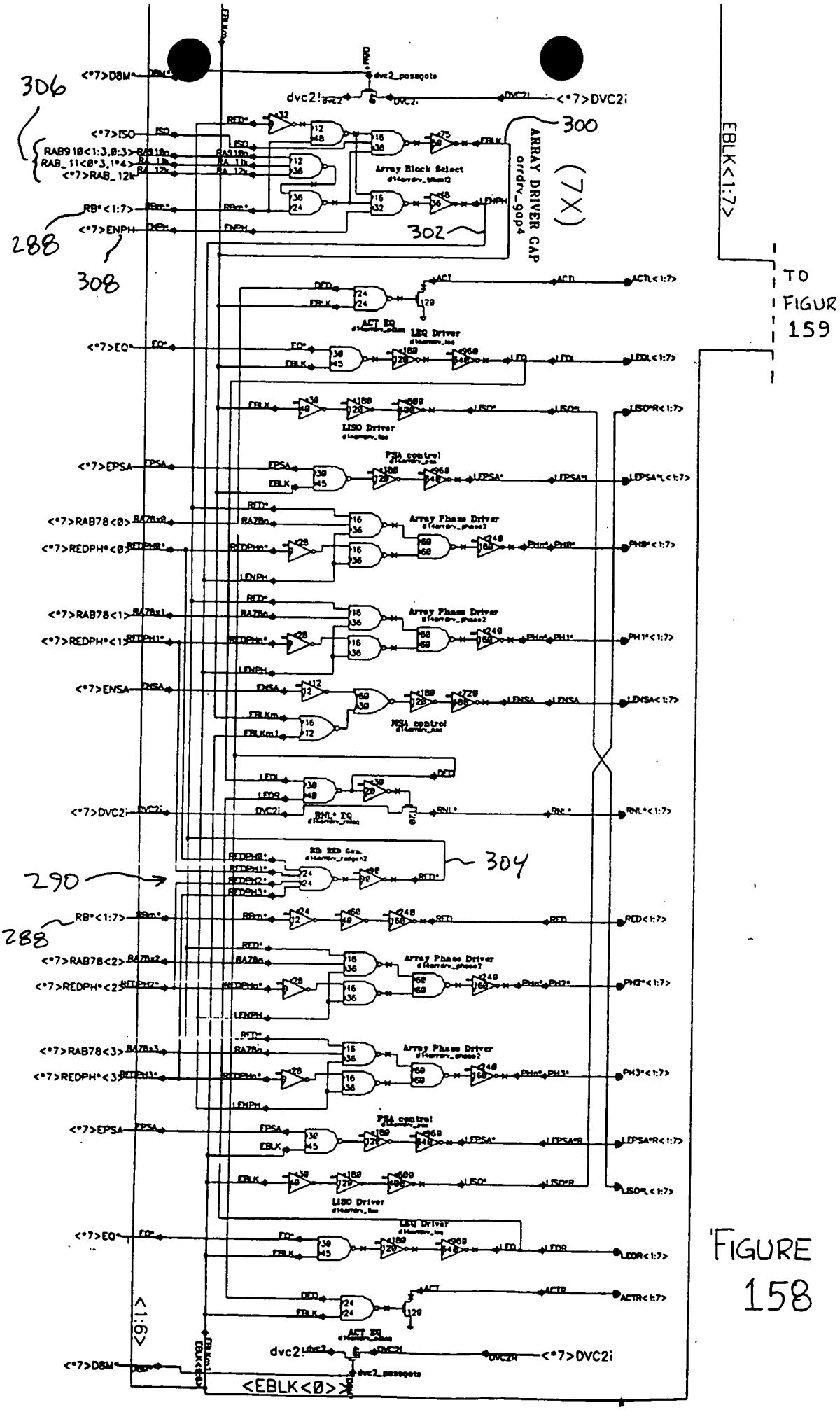
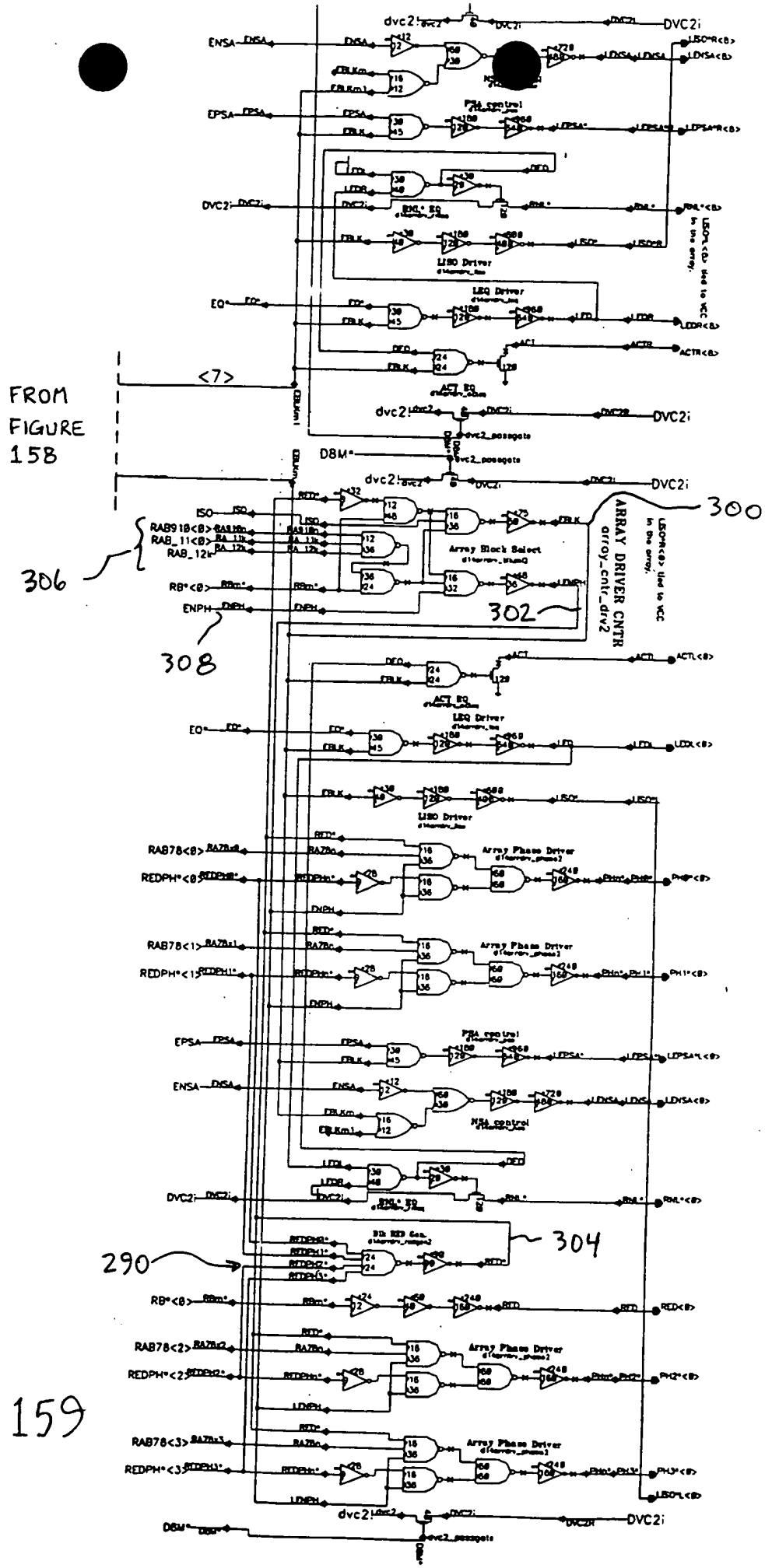

306
300
(7X)
ARRAY DRIVER GAP
arrdrv_gap4
Array Block Select
302
288
308
ACT EQ
LEQ Driver
LISO Driver
PSA control
Array Phase Driver
NSA control
RN1* EQ
304
290
EBLK<1:7>
TO FIGUR 159
<*7>D8M
<*7>DVC2i
<*7>ISO
RAB9 10<1:3,0:3>
RAB_11<0*3,1*4>
<*7>RAB_12k
RB*<1:7>
<*7>ENPH
<*7>EQ
<*7>EPSA
<*7>RAB78<0>
<*7>REDPH*<0>
<*7>RAB78<1>
<*7>REDPH*<1>
<*7>ENSA
<*7>RAB78<2>
<*7>REDPH*<2>
<*7>RAB78<3>
<*7>REDPH*<3>
<1:6>
<EBLK<0>>

FIGURE 158


FROM FIGURE 15B
<7>
306
308
300
302
290
304
ARRAY DRIVER CNTR
array_cntr_drv2
Array Block Select
LISO Driver
LEQ Driver
ACT EQ
Array Phase Driver
NSA control
PSA control
dvc2_passgate
DVC2i
DVC2
ISO
ENPH
EQ*
ACT
ACTR
ACTL
LISOR<0> tied to VCC in the array.

IGURE 159

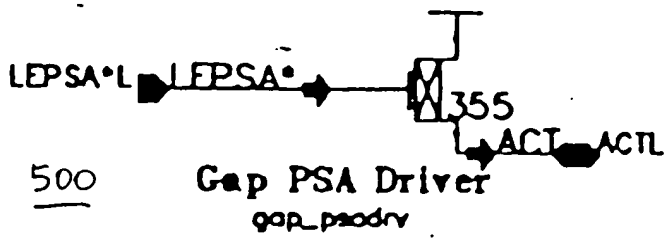


FIGURE 160

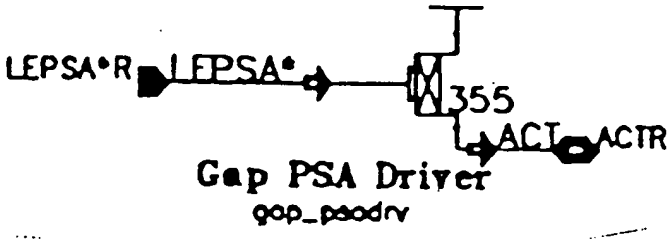


FIGURE 161

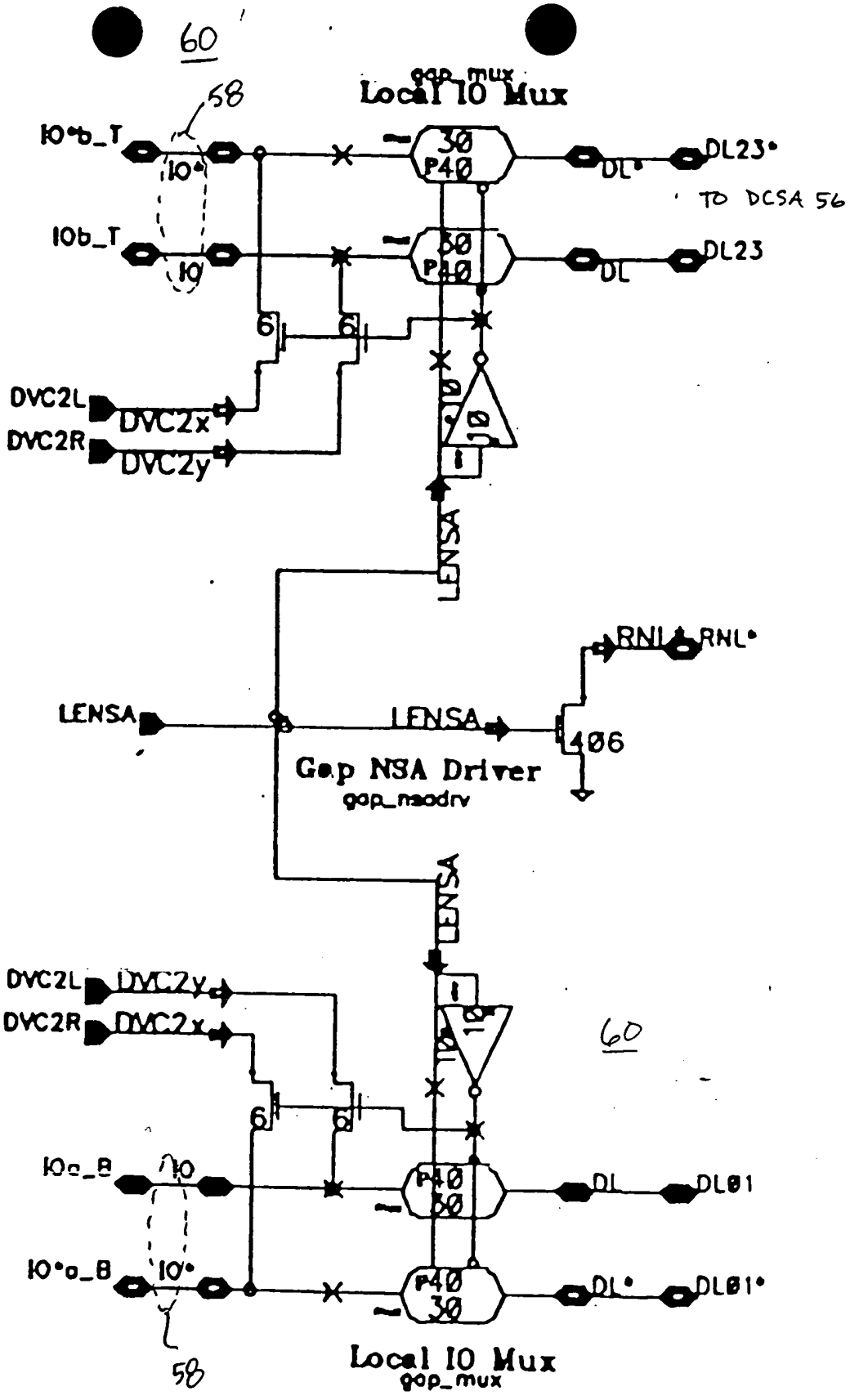

60
58
gap_mux
Local IO Mux
IO*b_T
IO*
IOb_T
IO
30
P40
DL*
DL23*
TO DCSA 56
DL
DL23
6
6
DVC2L
DVC2R
DVC2x
DVC2y
10
10
LENSA
RNL
RNL*
LENSA
LENSA
406
Gap NSA Driver
gap_nsadrv
LENSA
DVC2L
DVC2R
DVC2y
DVC2x
60
IOa_B
IO
P40
60
DL
DL01
IO*a_B
IO*
P40
30
DL*
DL01*
58
Local IO Mux
gap_mux

FIGURE 162

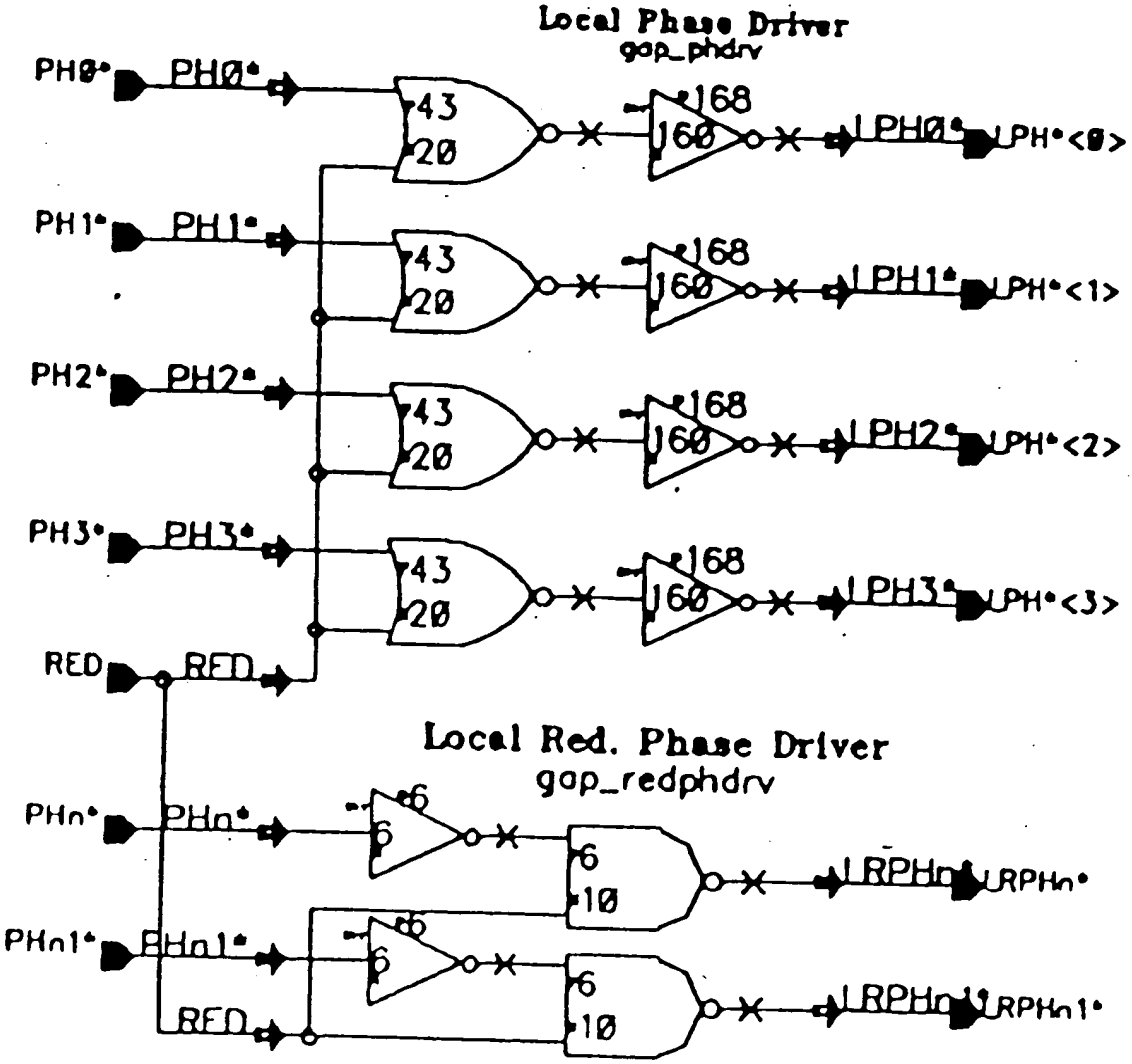

Local Phase Driver
gop_phdrv
PH0*
PH0*
43
20
168
160
LPH0*
LPH*<0>
PH1*
PH1*
43
20
168
160
LPH1*
LPH*<1>
PH2*
PH2*
43
20
168
160
LPH2*
LPH*<2>
PH3*
PH3*
43
20
168
160
LPH3*
LPH*<3>
RED
RED
Local Red. Phase Driver
gop_redphdrv
PHn*
PHn*
6
6
6
10
LRPHn
LRPHn*
PHn1*
PHn1*
6
6
6
10
LRPHn1
LRPHn1*
RED

FIGURE 163

INPUTS

OUTPUTS

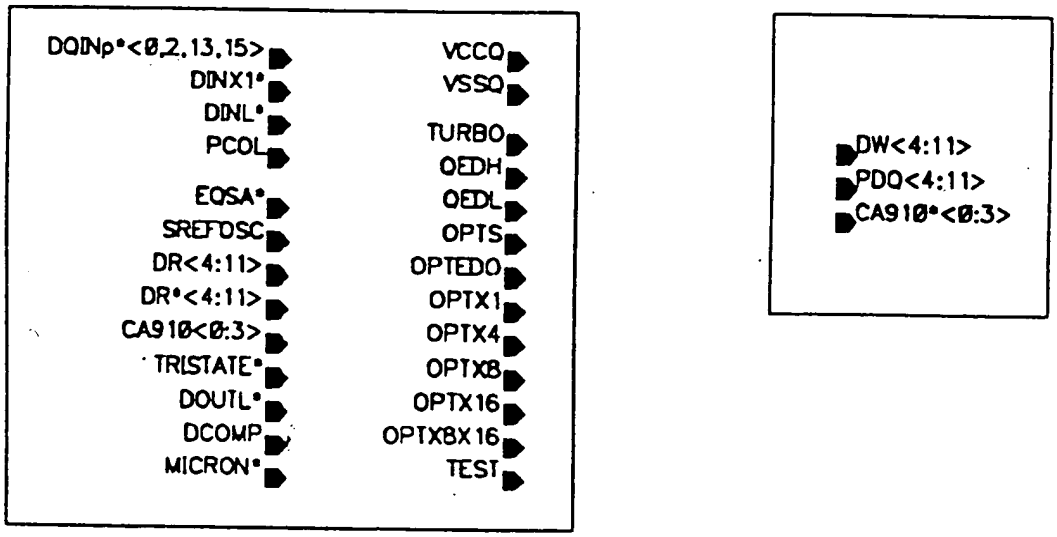


FIGURE 164

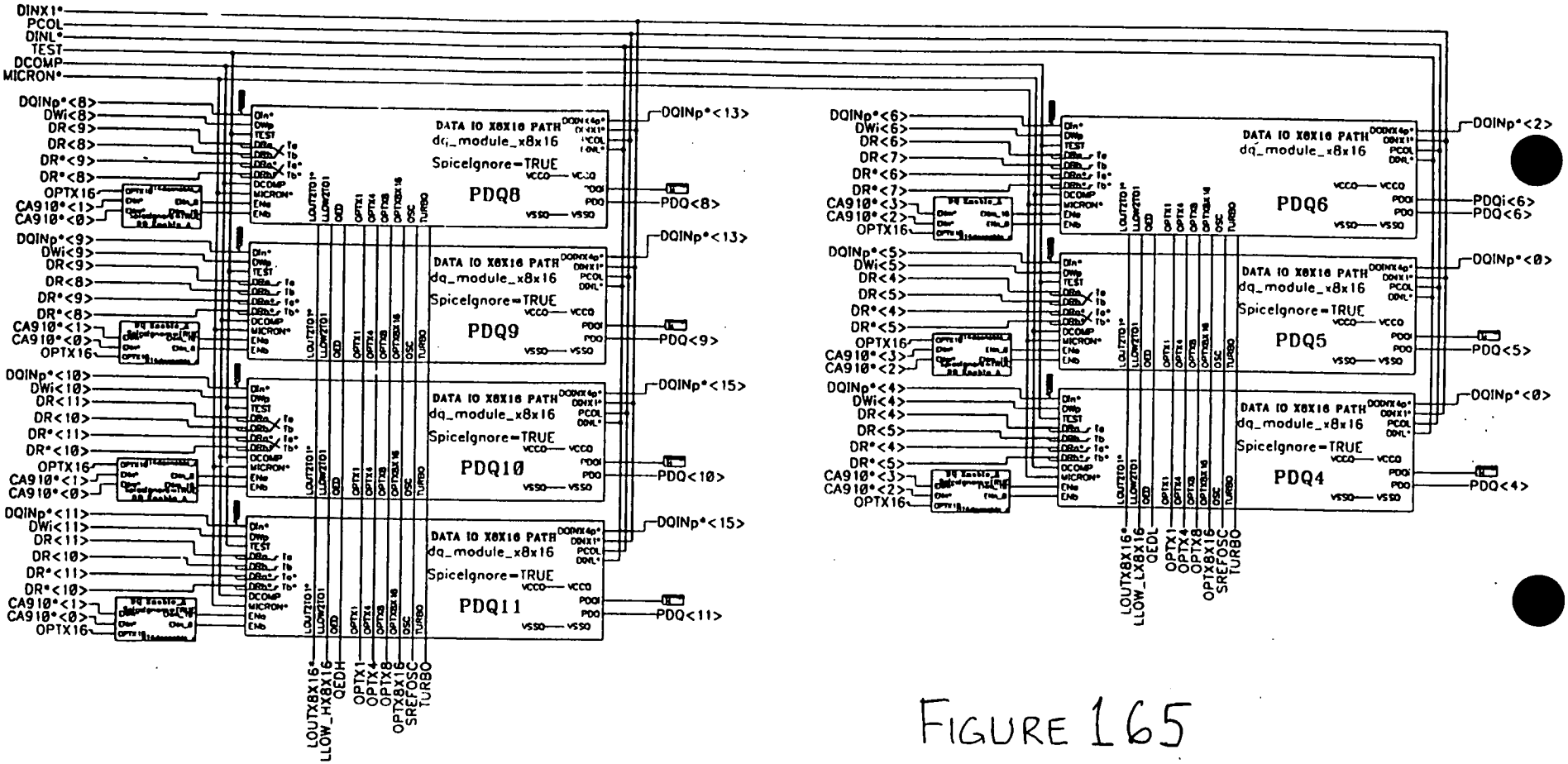

DINX1*
PCOL
DINL*
TEST
DCOMP
MICRON*
DQINp*<8>
DWi<8>
DR<9>
DR<8>
DR*<9>
DR*<8>
OPTX16
CA910*<1>
CA910*<0>
DQINp*<9>
DWi<9>
DR<9>
DR<8>
DR*<9>
DR*<8>
CA910*<1>
CA910*<0>
OPTX16
DQINp*<10>
DWi<10>
DR<11>
DR<10>
DR*<11>
DR*<10>
OPTX16
CA910*<1>
CA910*<0>
DQINp*<11>
DWi<11>
DR<11>
DR<10>
DR*<11>
DR*<10>
CA910*<1>
CA910*<0>
OPTX16
DATA IO X8X16 PATH
dq_module_x8x16
SpiceIgnore=TRUE
PDQ8
PDQ9
PDQ10
PDQ11
VCCO
VSSO
PDQI
PDO
DQINp*<13>
PDQ<8>
DQINp*<13>
PDQ<9>
DQINp*<15>
PDQ<10>
DQINp*<15>
PDQ<11>
LOUTX8X16*
LLOW_HX8X16
QEDH
OPTX1
OPTX4
OPTX8
OPTX8X16
SREFOSC
TURBO
DQINp*<6>
DWi<6>
DR<6>
DR<7>
DR*<6>
DR*<7>
CA910*<3>
CA910*<2>
OPTX16
DQINp*<5>
DWi<5>
DR<4>
DR<5>
DR*<4>
DR*<5>
OPTX16
CA910*<3>
CA910*<2>
DQINp*<4>
DWi<4>
DR<4>
DR<5>
DR*<4>
DR*<5>
CA910*<3>
CA910*<2>
OPTX16
PDQ6
PDQ5
PDQ4
DQINp*<2>
PDQi<6>
PDQ<6>
DQINp*<0>
PDQ<5>
DQINp*<0>
PDQ<4>
LOUTX8X16*
LLOW_LX8X16
QEDL
OPTX1
OPTX4
OPTX8
OPTX8X16
SREFOSC
TURBO

FIGURE 165

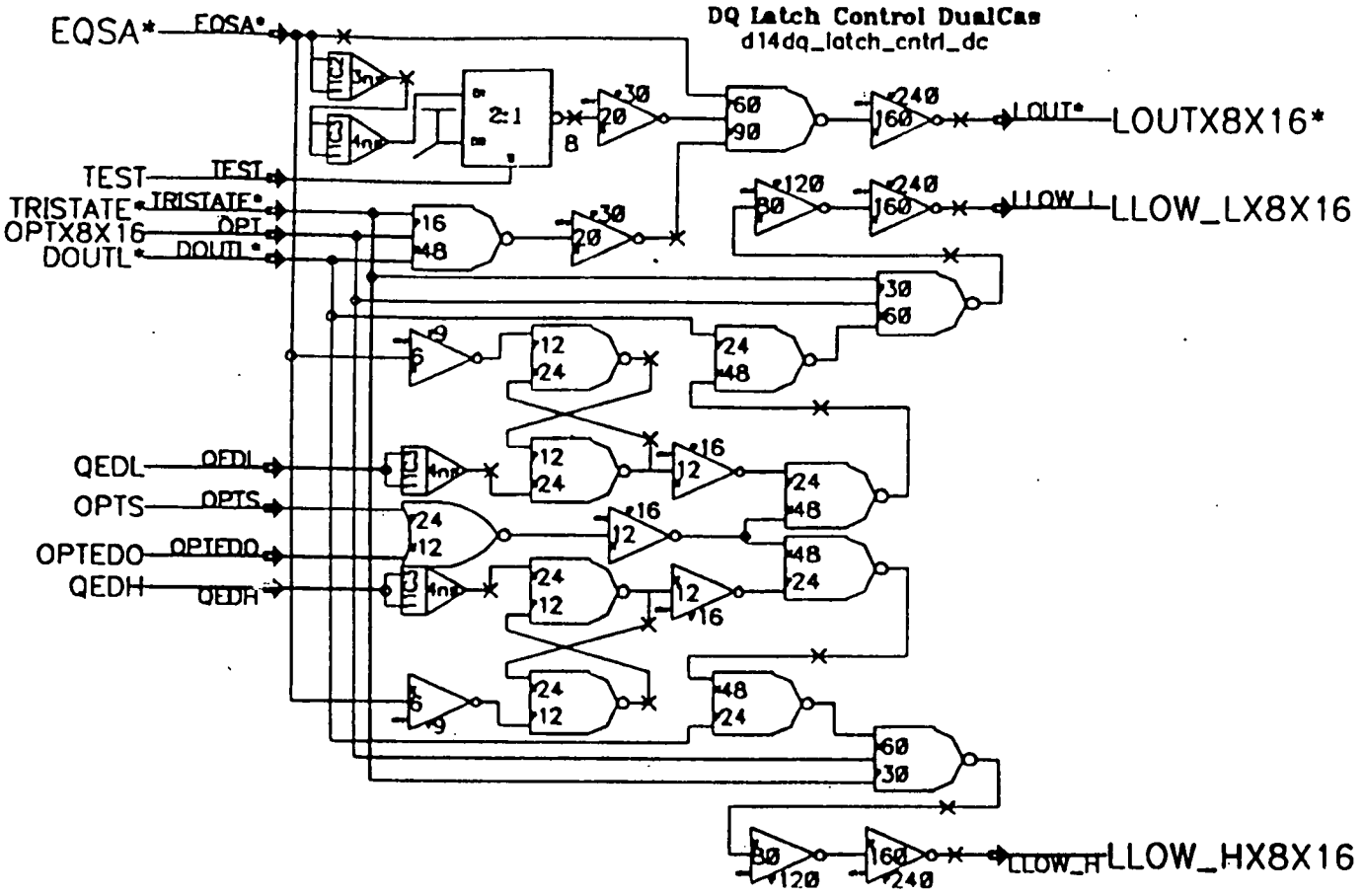

DQ Latch Control DualCas
d14dq_latch_cntrl_dc
EQSA*
EQSA*
TEST
TEST
TRISTATE*
IRISTATE*
OPTX8X16
OPT
DOUTL*
DOUTL*
QEDL
QEDL
OPTS
OPTS
OPTEDO
OPTEDO
QEDH
QEDH
2:1
8
LOUT*
LOUTX8X16*
LLOW_L
LLOW_LX8X16
LLOW_H
LLOW_HX8X16

FIGURE 166

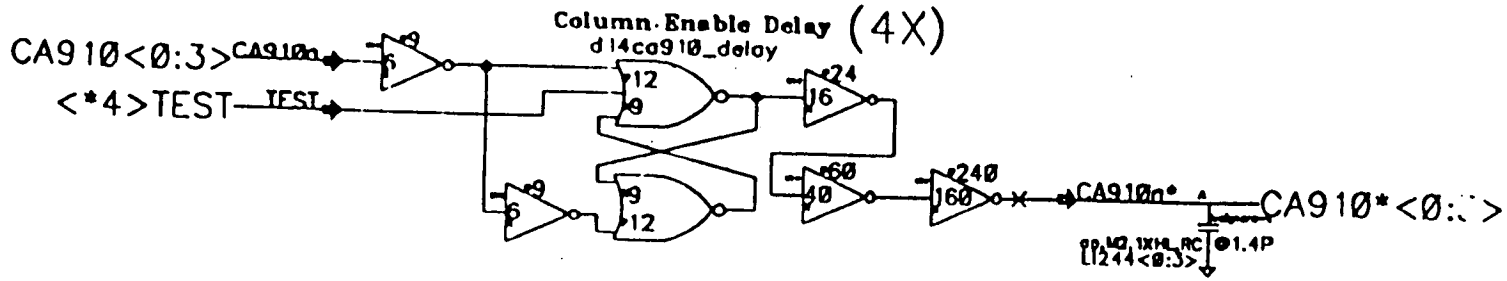

Column Enable Delay (4X)
d14ca910_delay
CA910<0:3>
CA910n
<*4>TEST
TEST
9
6
12
9
24
16
9
6
9
12
60
40
240
160
CA910n*
CA910*<0:3>
1.4P

FIGURE 167

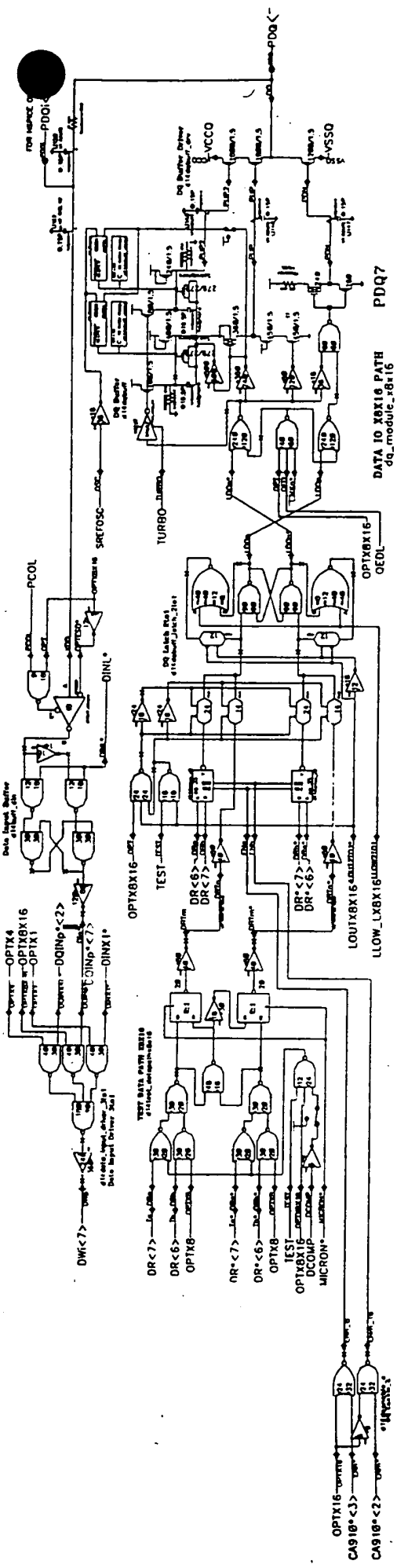

PDQ7
DATA IO X8X16 PATH
dq_module_x8x16
VCCO
VSSO
TURBO
SREFOSC
PCOL
OINL*
OPTX8X16
TEST
DR<6>
DR<7>
DR*<7>
DR*<6>
LOUTX8X16
LLOW_LX8X16
OPTX4
OPTX8X16
OPTX1
DQINp*<2>
DQINp*<7>
DINX1*
DWr<7>
OPTX8
OPTX16
CA910*<3>
CA910*<2>

FIGURE 168

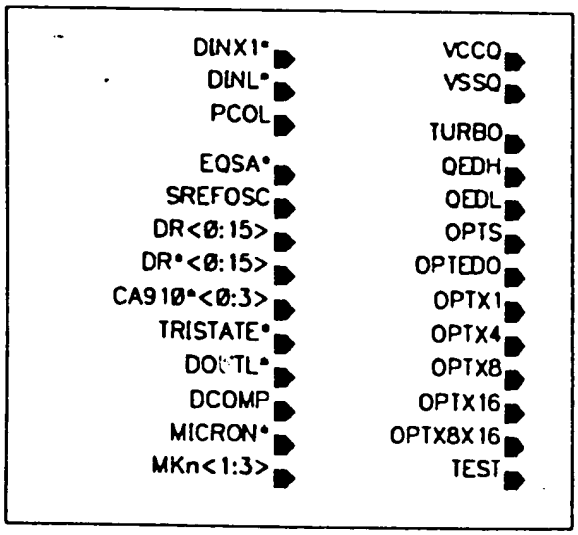
X8/X16 DQ Pads

(DQ4 DQ5 DQ6 DQ7 DQ8 DQ9 DQ10 DQ11)

Assembly Pin-out	Schematic Pin-out	Bond Pad PDQ	DW	DR/DR*
DQ1	DQ0	0 1	0 1	0, 1 0, 1
DQ2	DQ1	2 3	2 3	2, 3 2, 3
DQ3	DQ2	4 5	4 5	4, 5 4, 5
DQ4	DQ3	6 7	6 7	6, 7 6, 7
DQ5	DQ4	8 9	8 9	8, 9 8, 9
DQ6	DQ5	10 11	10 11	10, 11 10, 11
DQ7	DQ6	12 13	12 13	12, 13 12, 13
DQ8	DQ7	14 15	14 15	14, 15 14, 15

FIGURE 169

INPUTS



OUTPUTS

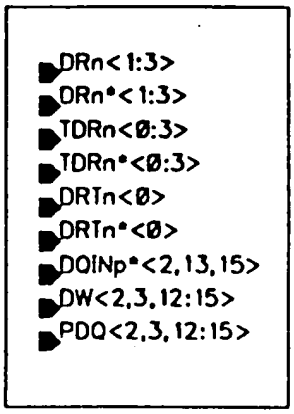


FIGURE 170

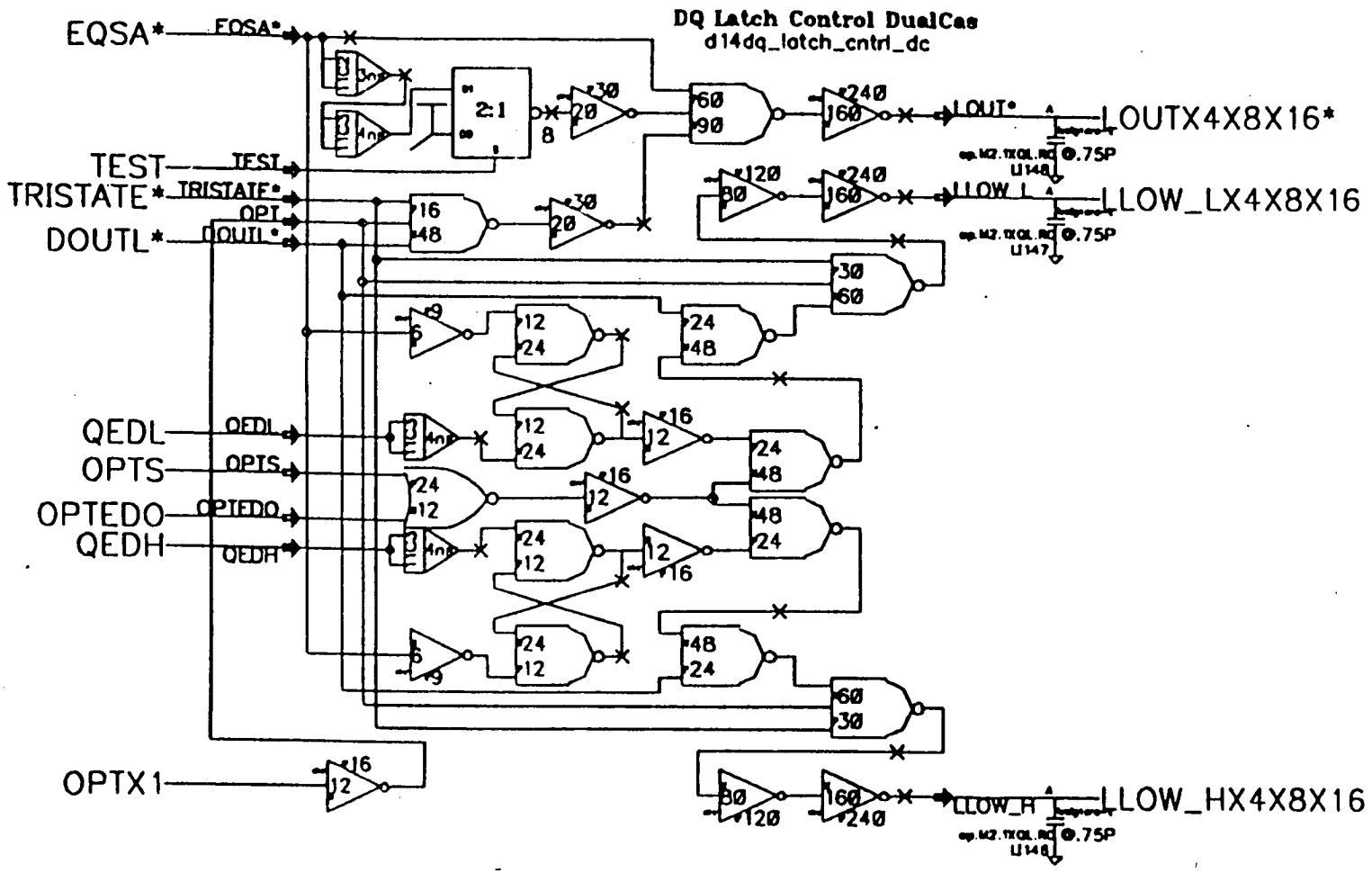

DQ Latch Control DualCas
d14dq_latch_cntrl_dc
EQSA*
EQSA*
TEST
TEST
TRISTATE*
TRISTATE*
OPT
DOUTL*
DOUTL*
QEDL
QEDL
OPTS
OPTS
OPTEDO
OPTEDO
QEDH
QEDH
OPTX1
2:1
LOUT*
LOUTX4X8X16*
LLOW_L
LLOW_LX4X8X16
LLOW_H
LLOW_HX4X8X16

FIGURE 171

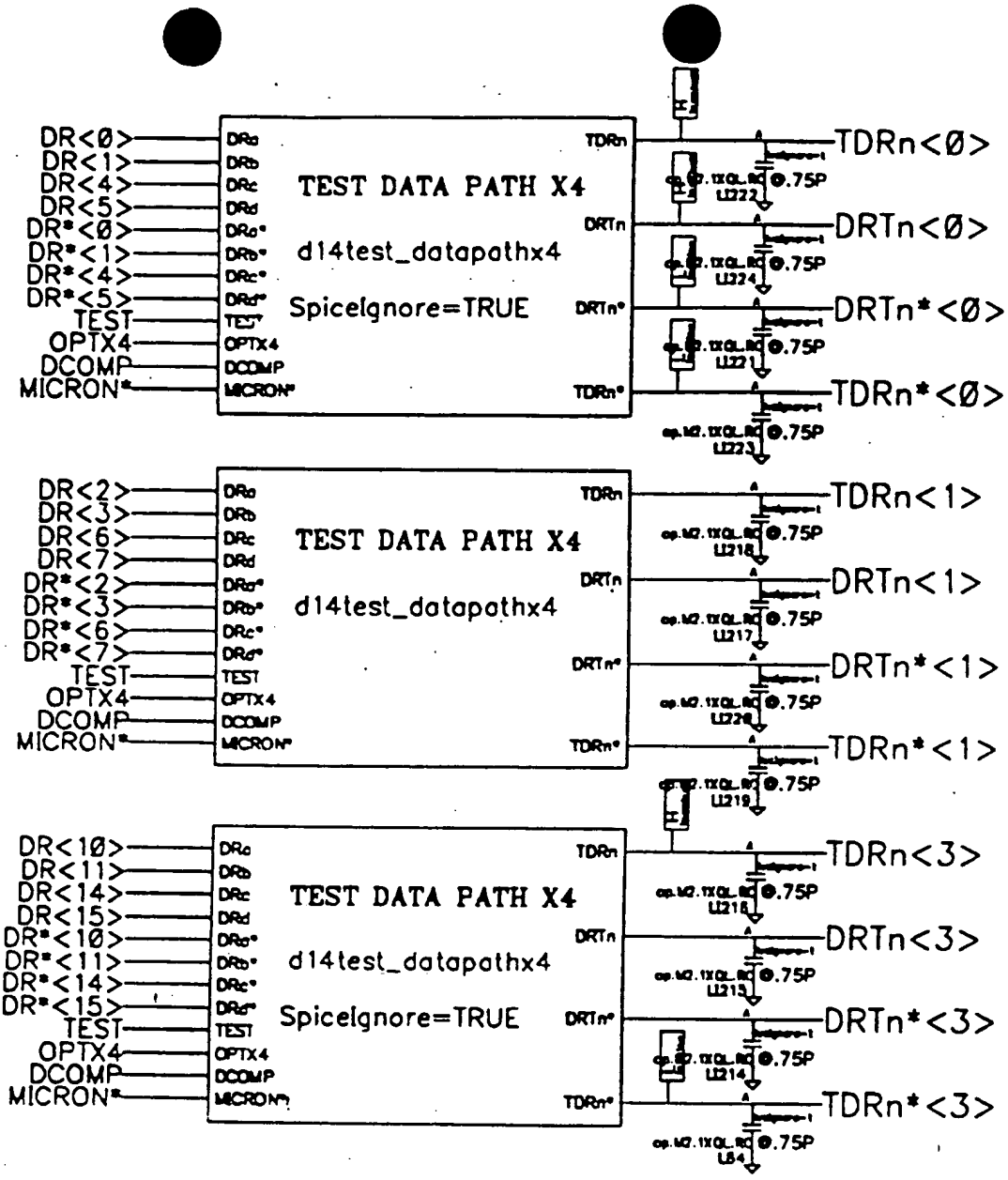

DR<0>
DR<1>
DR<4>
DR<5>
DR*<0>
DR*<1>
DR*<4>
DR*<5>
TEST
OPTX4
DCOMP
MICRON*
TEST DATA PATH X4
d14test_datapathx4
SpiceIgnore=TRUE
TDRn<0>
DRTn<0>
DRTn*<0>
TDRn*<0>
DR<2>
DR<3>
DR<6>
DR<7>
DR*<2>
DR*<3>
DR*<6>
DR*<7>
TDRn<1>
DRTn<1>
DRTn*<1>
TDRn*<1>
DR<10>
DR<11>
DR<14>
DR<15>
DR*<10>
DR*<11>
DR*<14>
DR*<15>
TDRn<3>
DRTn<3>
DRTn*<3>
TDRn*<3>

FIGURE 172

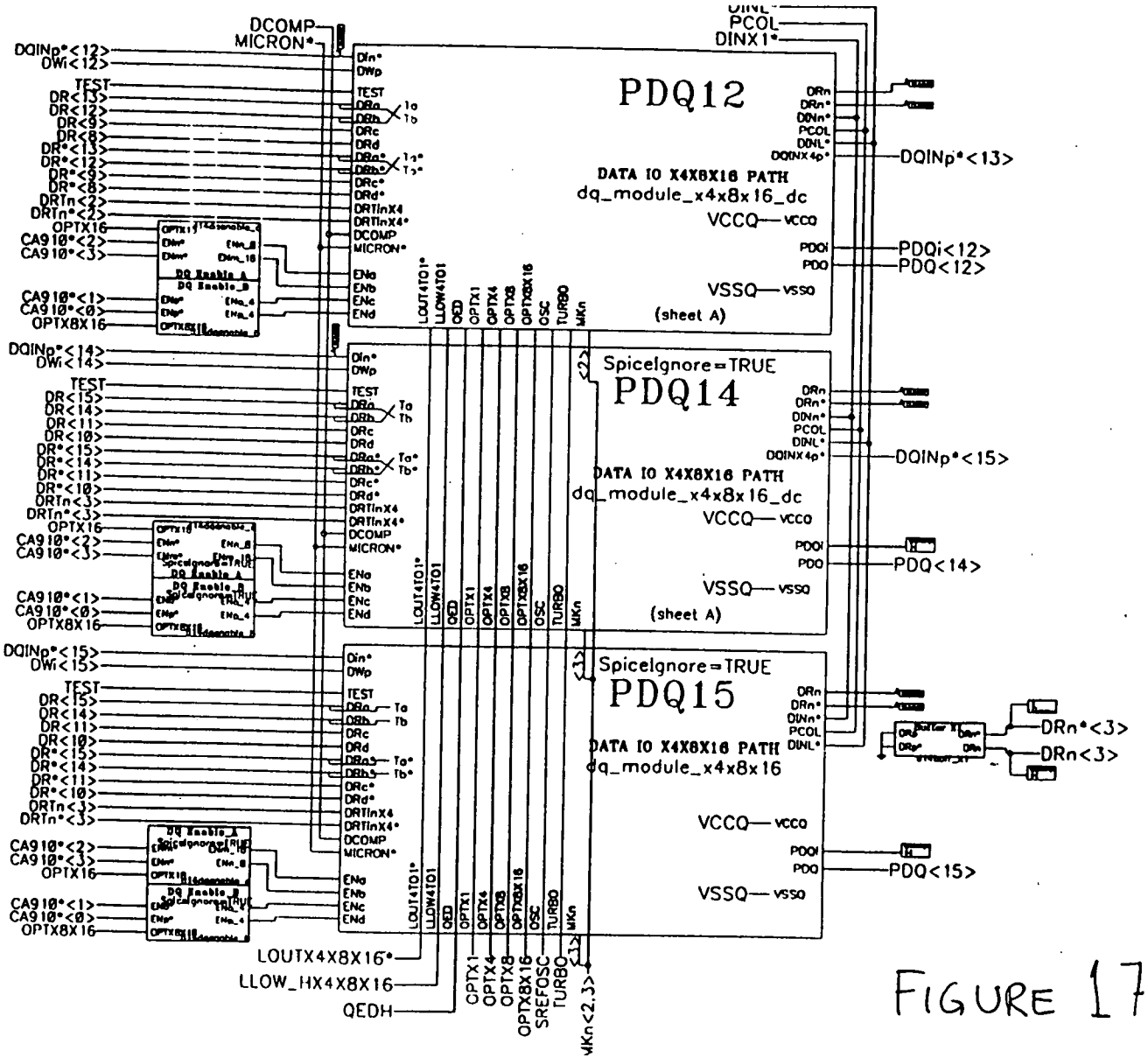

PDQ12
DATA IO X4X8X16 PATH
dq_module_x4x8x16_dc
(sheet A)
PDQ14
SpiceIgnore=TRUE
DATA IO X4X8X16 PATH
dq_module_x4x8x16_dc
(sheet A)
PDQ15
SpiceIgnore=TRUE
DATA IO X4X8X16 PATH
dq_module_x4x8x16
VCCQ
VSSQ
DCOMP
MICRON*
PCOL
DINX1*
DQINp*<13>
PDQi<12>
PDQ<12>
DQINp*<15>
PDQ<14>
DRn*<3>
DRn<3>
PDQ<15>
LOUTX4X8X16*
LLOW_HX4X8X16
QEDH
OPTX1
OPTX4
OPTX8
OPTX8X16
SREFOSC
TURBO
WKn<2.3>

FIGURE 173

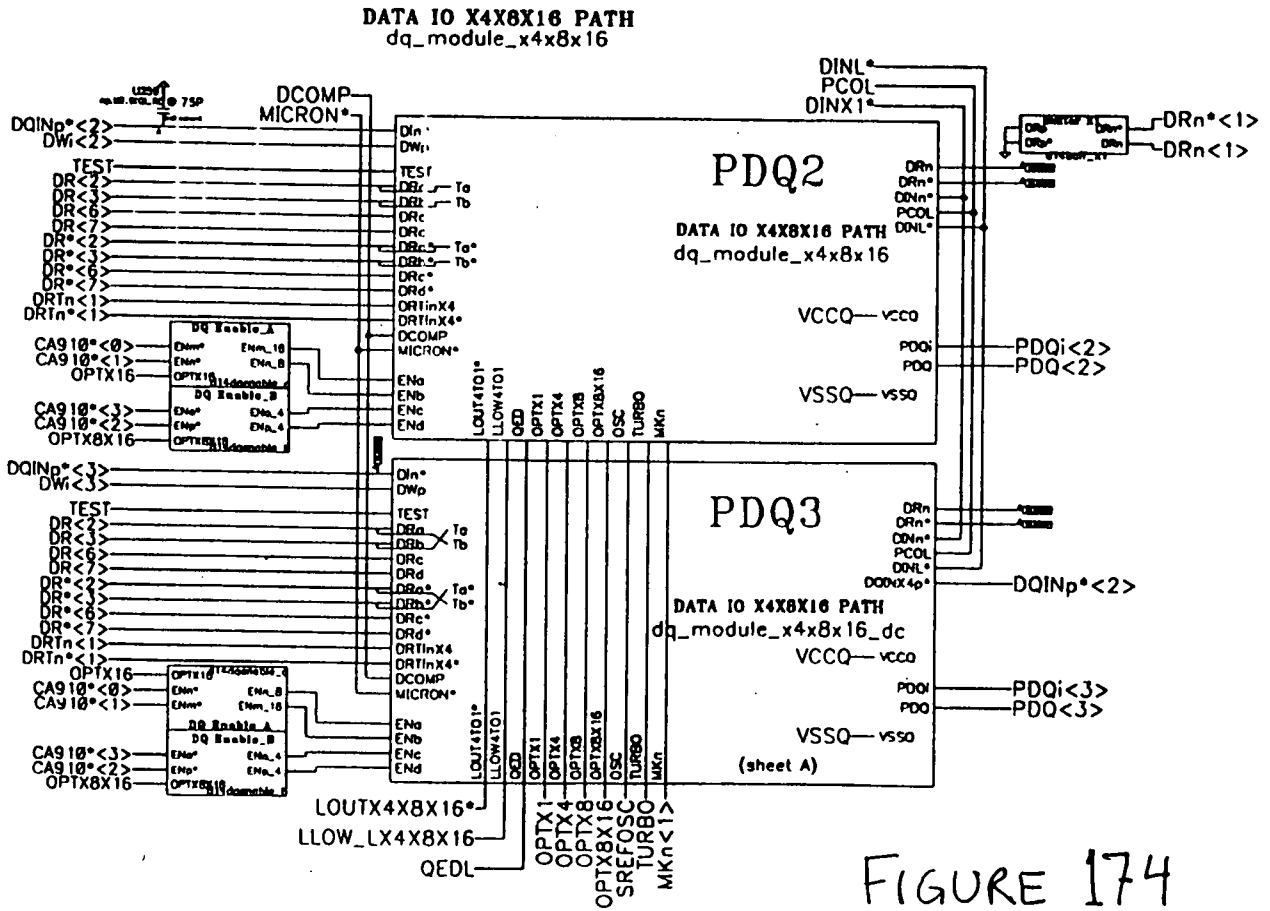

DATA IO X4X8X16 PATH
dq_module_x4x8x16
PDQ2
DATA IO X4X8X16 PATH
dq_module_x4x8x16
PDQ3
DATA IO X4X8X16 PATH
dq_module_x4x8x16_dc
(sheet A)
DINL*
PCOL
DINX1*
DCOMP
MICRON*
DRn*<1>
DRn<1>
PDQi<2>
PDQ<2>
DQINp*<2>
PDQi<3>
PDQ<3>
LOUTX4X8X16*
LLOW_LX4X8X16
QEDL
OPTX1
OPTX4
OPTX8
OPTX8X16
SREFOSC
TURBO
MKn<1>

FIGURE 174

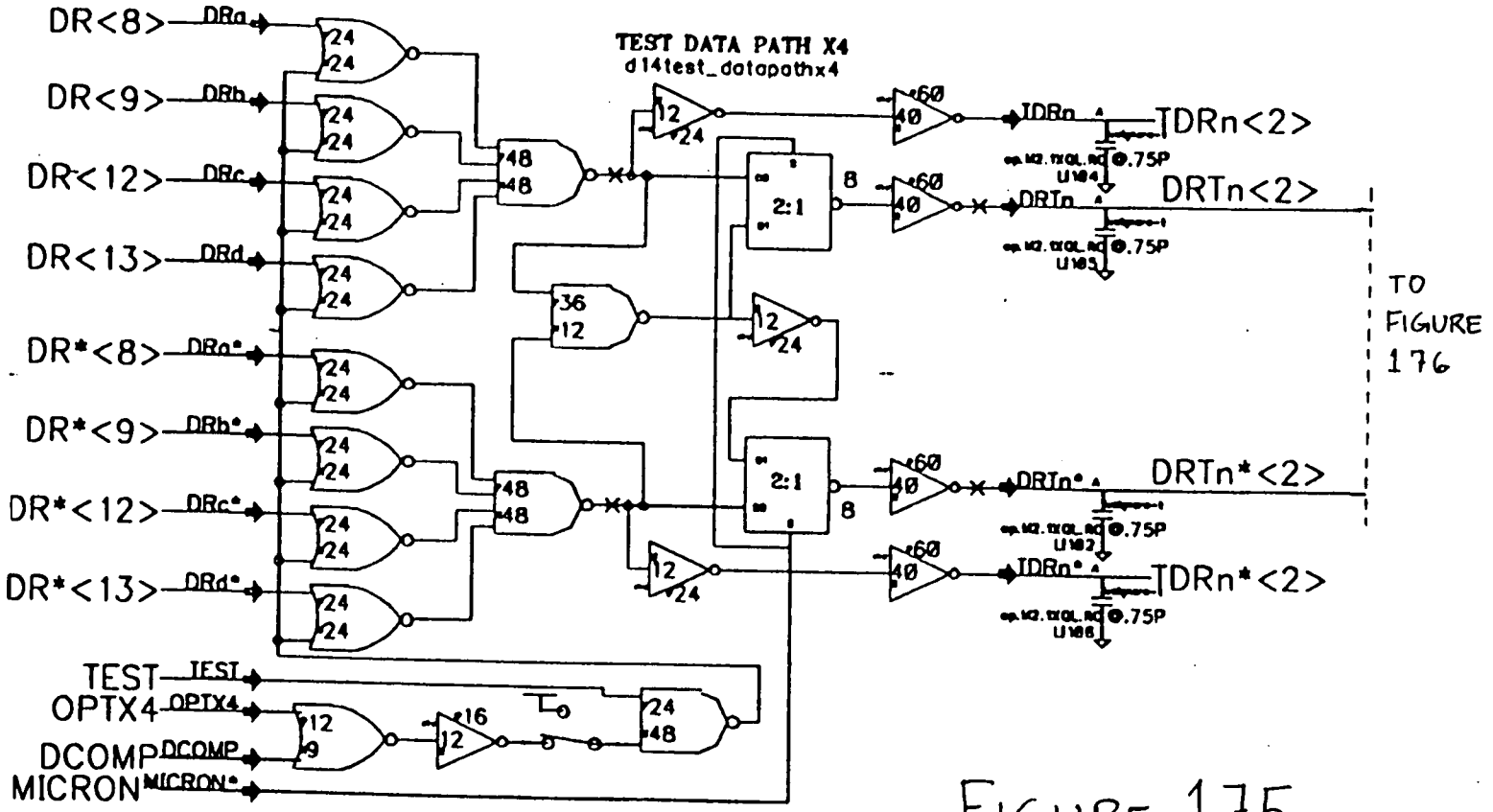

TEST DATA PATH X4
d14test_datapathx4
DR<8>
DR<9>
DR<12>
DR<13>
DR*<8>
DR*<9>
DR*<12>
DR*<13>
TEST
OPTX4
DCOMP
MICRON
DRTn<2>
DRTn*<2>
TO FIGURE 176

FIGURE 175

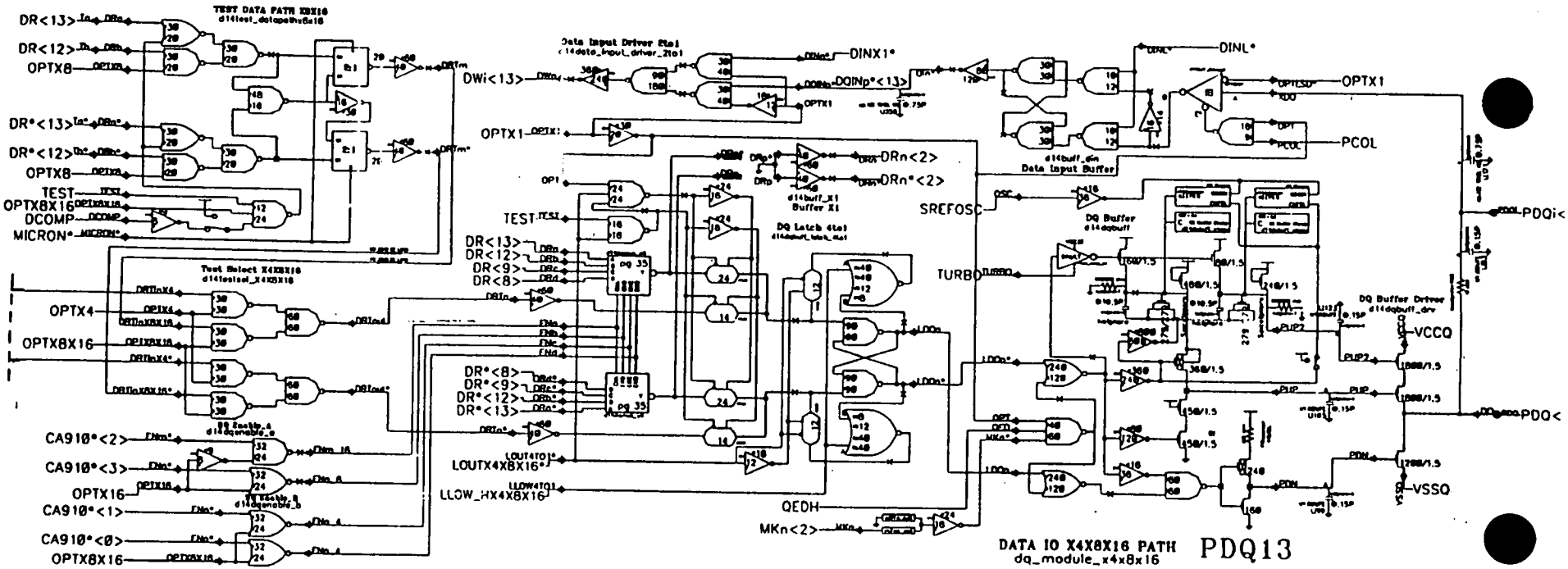

FROM FIGURE 175
DR<13>
DR<12>
OPTX8
DR*<13>
DR*<12>
OPTX8
TEST
OPTX8X16
DCOMP
MICRON*
OPTX4
OPTX8X16
CA910*<2>
CA910*<3>
OPTX16
CA910*<1>
CA910*<0>
OPTX8X16
DWi<13>
OPTX1
DR<13>
DR<12>
DR<9>
DR<8>
DR*<8>
DR*<9>
DR*<12>
DR*<13>
LOUTX4X8X16*
LLOW_HX4X8X16
QEDH
MKn<2>
DINX1*
DINL*
OPTX1
PCOL
SREFOSC
TURBO
ORn<2>
ORn*<2>
VCCO
VSSQ
PDQi<
PDQ<
DATA IO X4X8X16 PATH
dq_module_x4x8x16
PDQ13

FIGURE 176

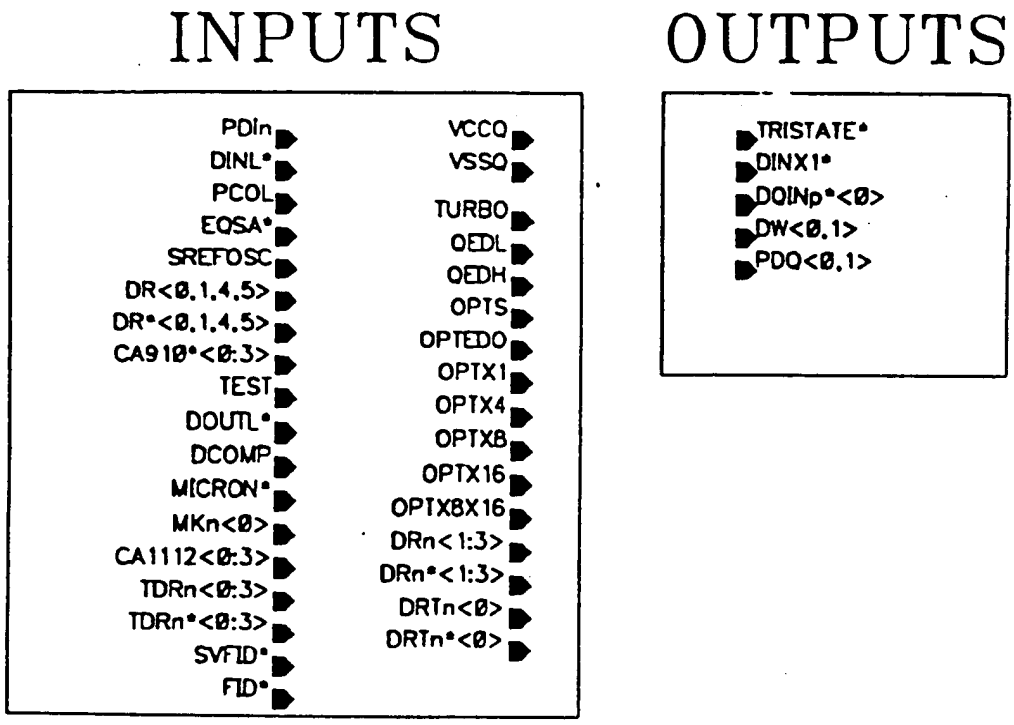

INPUTS
OUTPUTS
PDIn
DINL*
PCOL
EQSA*
SREFOSC
DR<0,1,4,5>
DR*<0,1,4,5>
CA910*<0:3>
TEST
DOUTL*
DCOMP
MICRON*
MKn<0>
CA1112<0:3>
TDRn<0:3>
TDRn*<0:3>
SVFID*
FID*
VCCQ
VSSQ
TURBO
OEDL
OEDH
OPTS
OPTEDO
OPTX1
OPTX4
OPTX8
OPTX16
OPTX8X16
DRn<1:3>
DRn*<1:3>
DRTn<0>
DRTn*<0>
TRISTATE*
DINX1*
DOINp*<0>
DW<0,1>
PDQ<0,1>

FIGURE 177

X4 Configuration

Assembly Pin-out	Schematic Pin-out	Bond Pad PDQ	Data Write DW	Data Read DR/DR*
DQ1	DQ0	0	0, 4, 5	0, 1, 4, 5
		1	1	0, 1, 4, 5
DQ2	DQ1	2	2, 6, 7	2, 3, 6, 7
		3	3	2, 3, 6, 7
DQ3	DQ2	12	12	8, 9, 12, 13
		13	13, 8, 9	8, 9, 12, 13
DQ4	DQ3	14	14	10, 11, 14, 15
		15	15, 10, 11	10, 11, 14, 15

X1 Configuration (see next page)

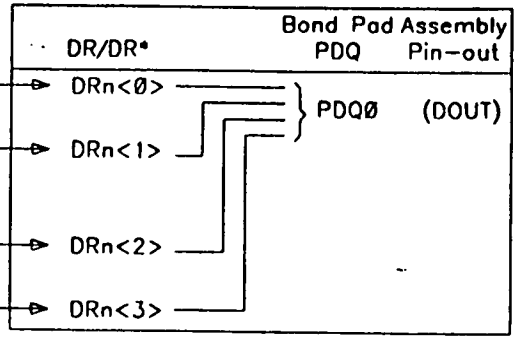


FIGURE 178

DQ Compression

DR/DW	PDQ	X8 DQ	X16 DQ
0,1,4,5	0,1	0	0
2,3,6,7	2,3	1	2
8,9,12,13	12,13	6	13
10,11,14,15	14,15	7	15

FIGURE 179

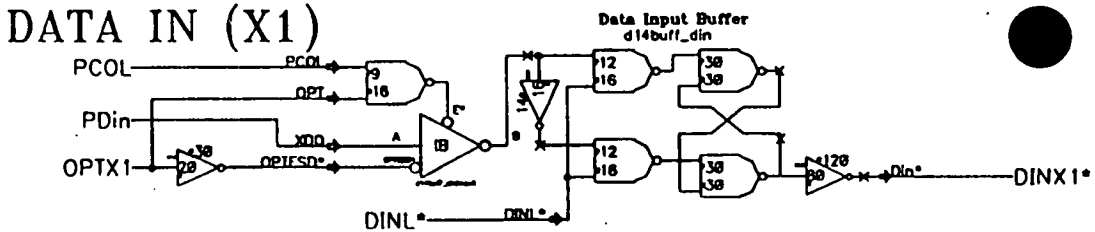


FIGURE 180

614

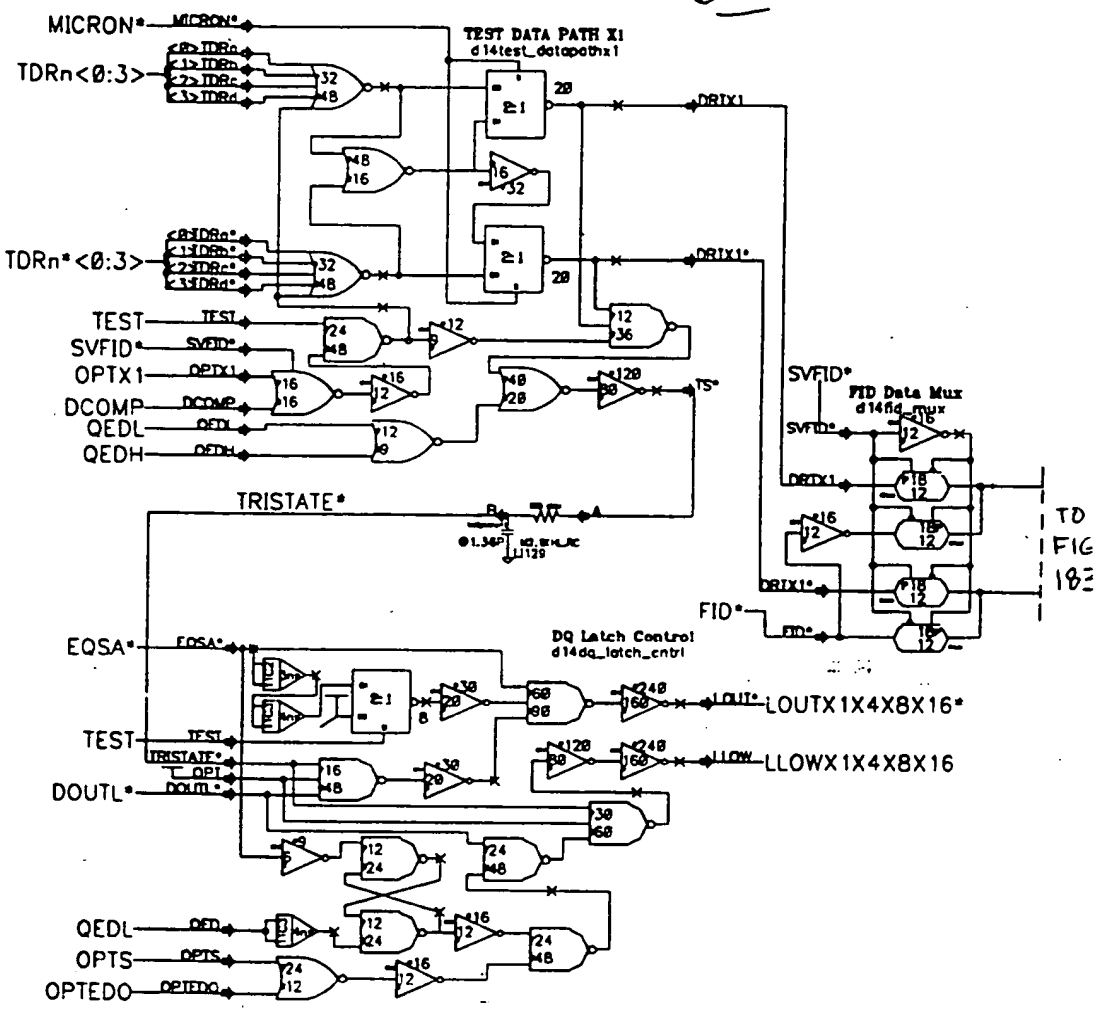


FIGURE 182

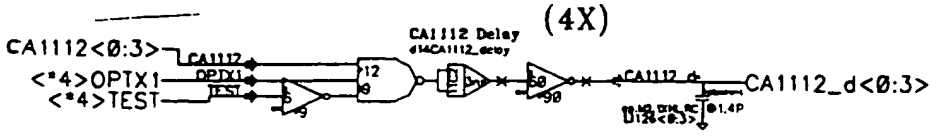


FIGURE 181

614

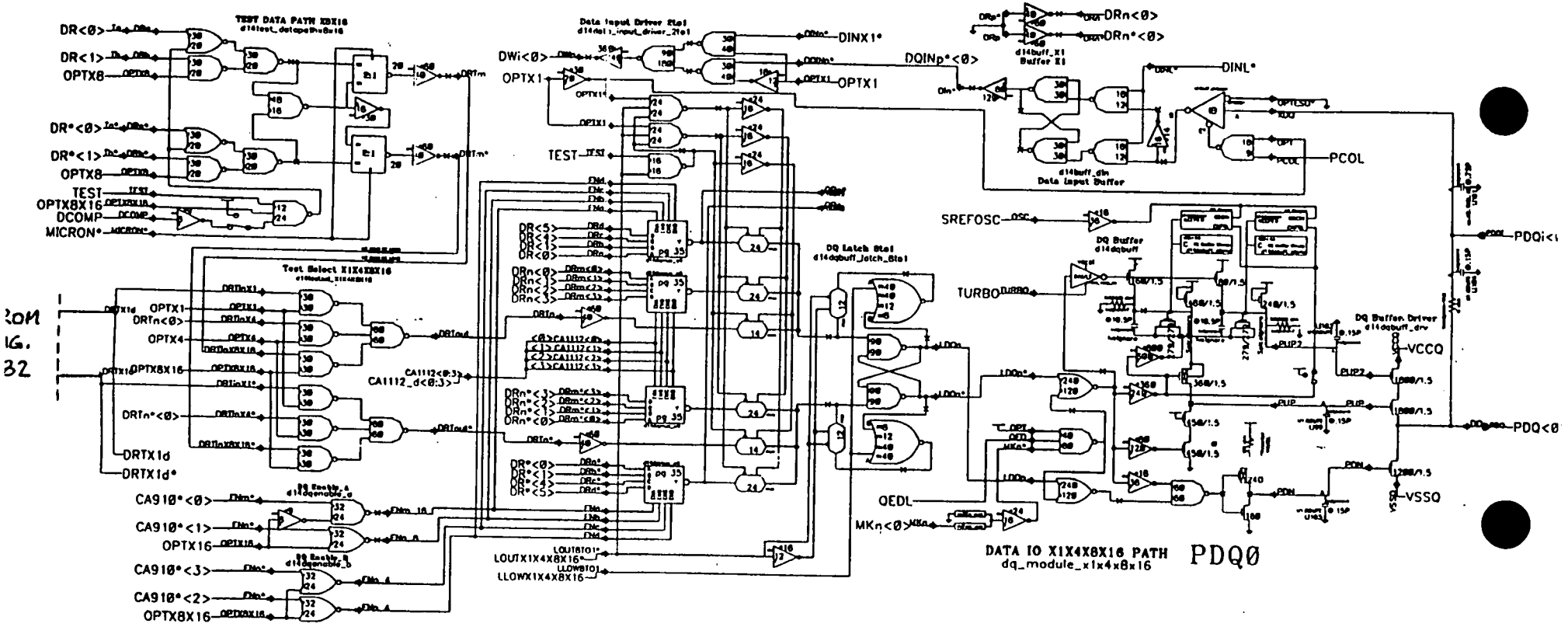
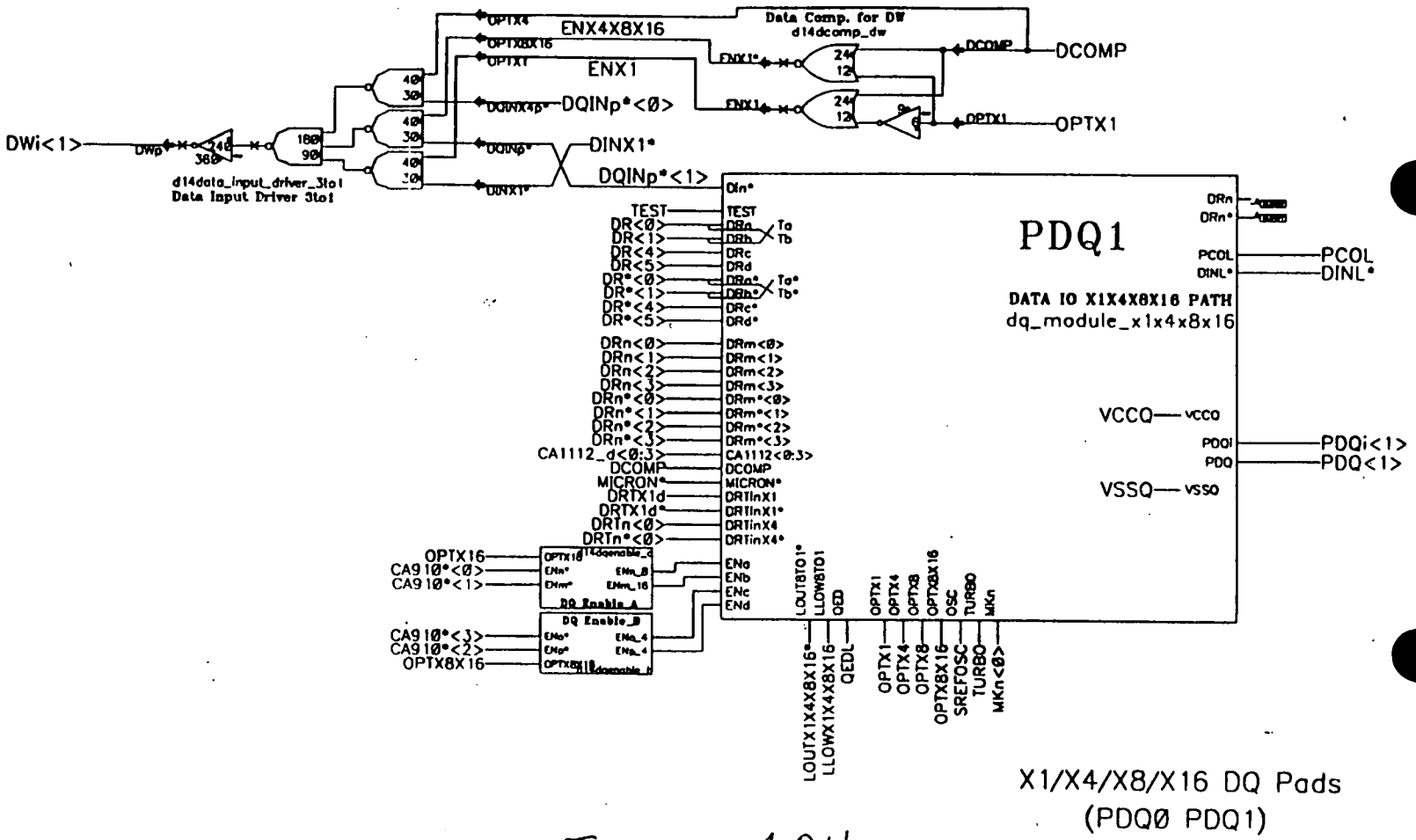


FIGURE 183



X1/X4/X8/X16 DQ Pads
(PDQ0 PDQ1)

FIGURE 184

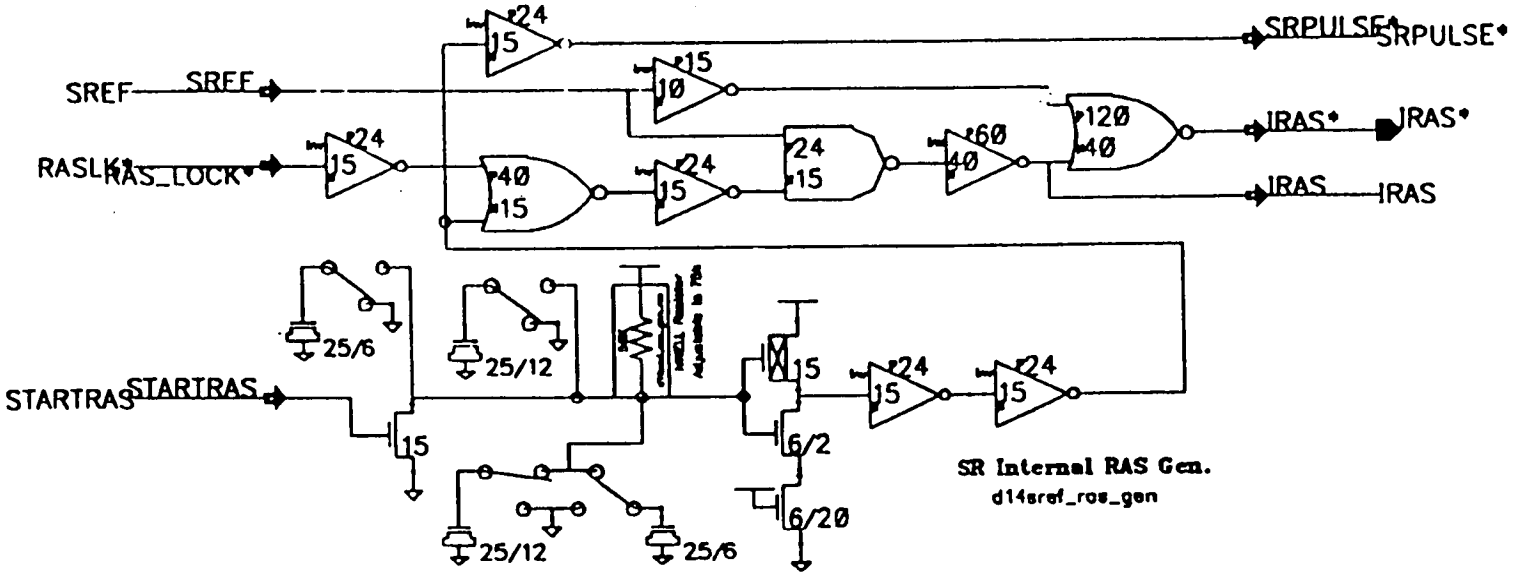

SREF
SREF
RASLK1
RAS_LOCK*
STARTRAS
STARTRAS
SRPULSE
SRPULSE*
IRAS*
IRAS*
IRAS
IRAS
24/15
15/10
24/15
40/15
24/15
60/40
120/40
24/15
24/15
25/6
25/12
15
6/2
6/20
25/12
25/6
SR Internal RAS Gen.
d14sref_ros_gen

FIGURE 185

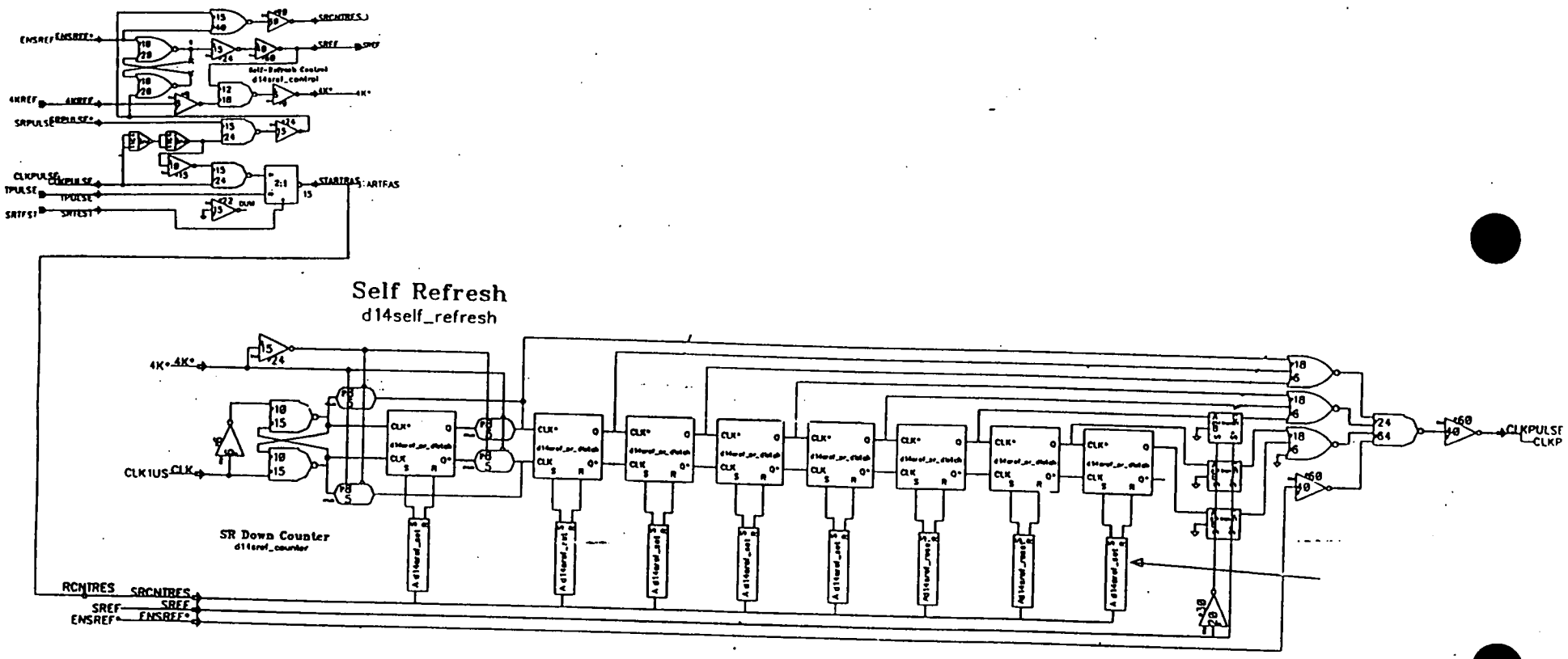

Self Refresh
d14self_refresh
SR Down Counter
d14sref_counter
ENSREF
4KREF
SRPULSE
CLKPULSE
TPULSE
SRTEST
STARTRAS
ARTFAS
4K*
CLK1US
CLK
RCNTRES
SRCNTRES
SREF
ENSREF*
CLKPULSE
CLKP

FIGURE 186

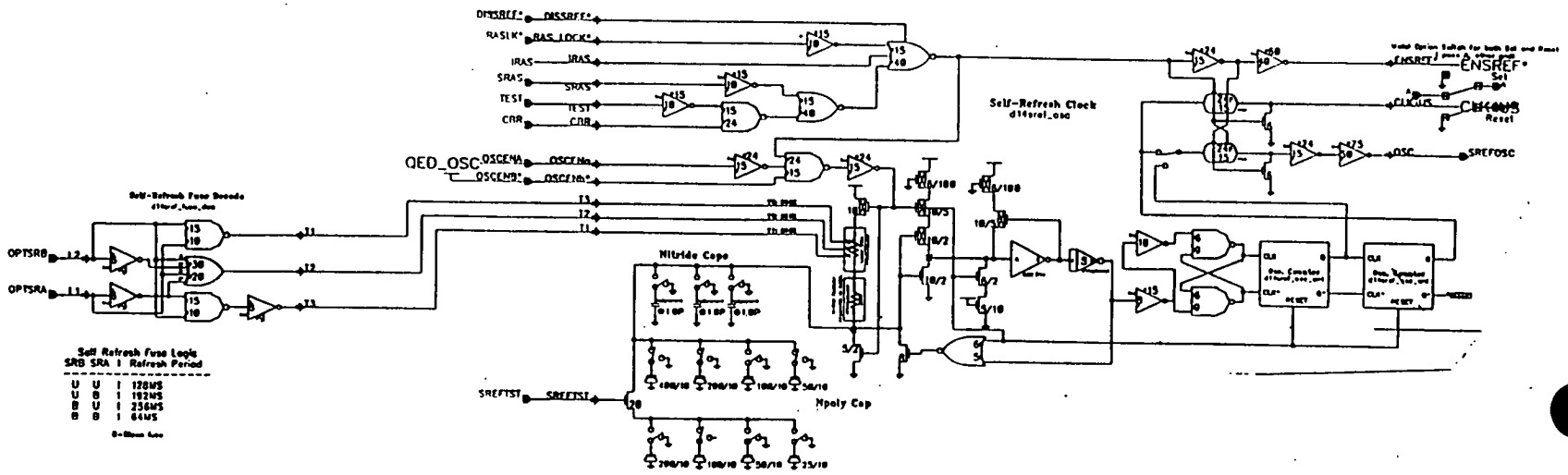

QED_OSC
OPTSRB
OPTSRA
RASLK*
IRAS
SRAS
TEST
CNR
OSCENA
OSCENB*
SREFTST
Nitride Cap
Npoly Cap
Self-Refresh Clock
d14srel_osc
ENSREF*
CLKOUS
OSC
SREFOSC
Self Refresh Fuse Logic
SRB SRA | Refresh Period
0 0 | 128MS
0 1 | 192MS
1 0 | 256MS
1 1 | 64MS

FIGURE 187

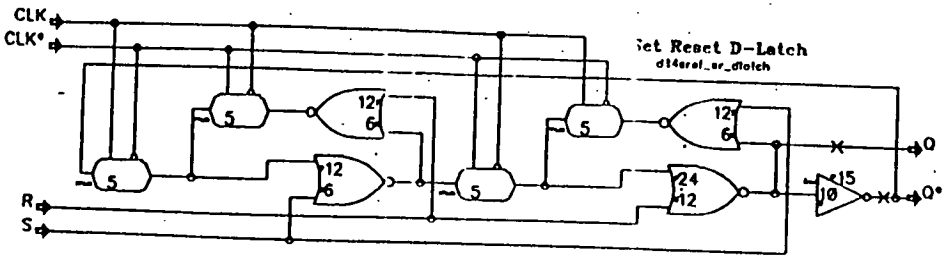


FIGURE 188

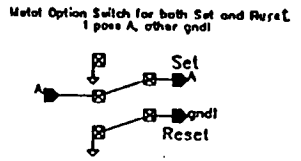


FIGURE 189

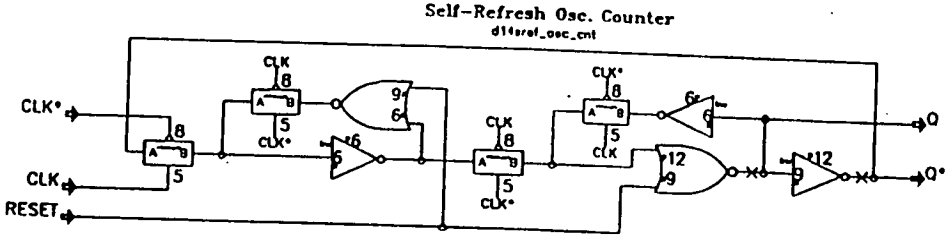


FIGURE 190

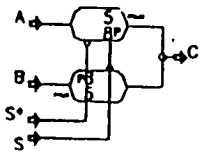


FIGURE 191

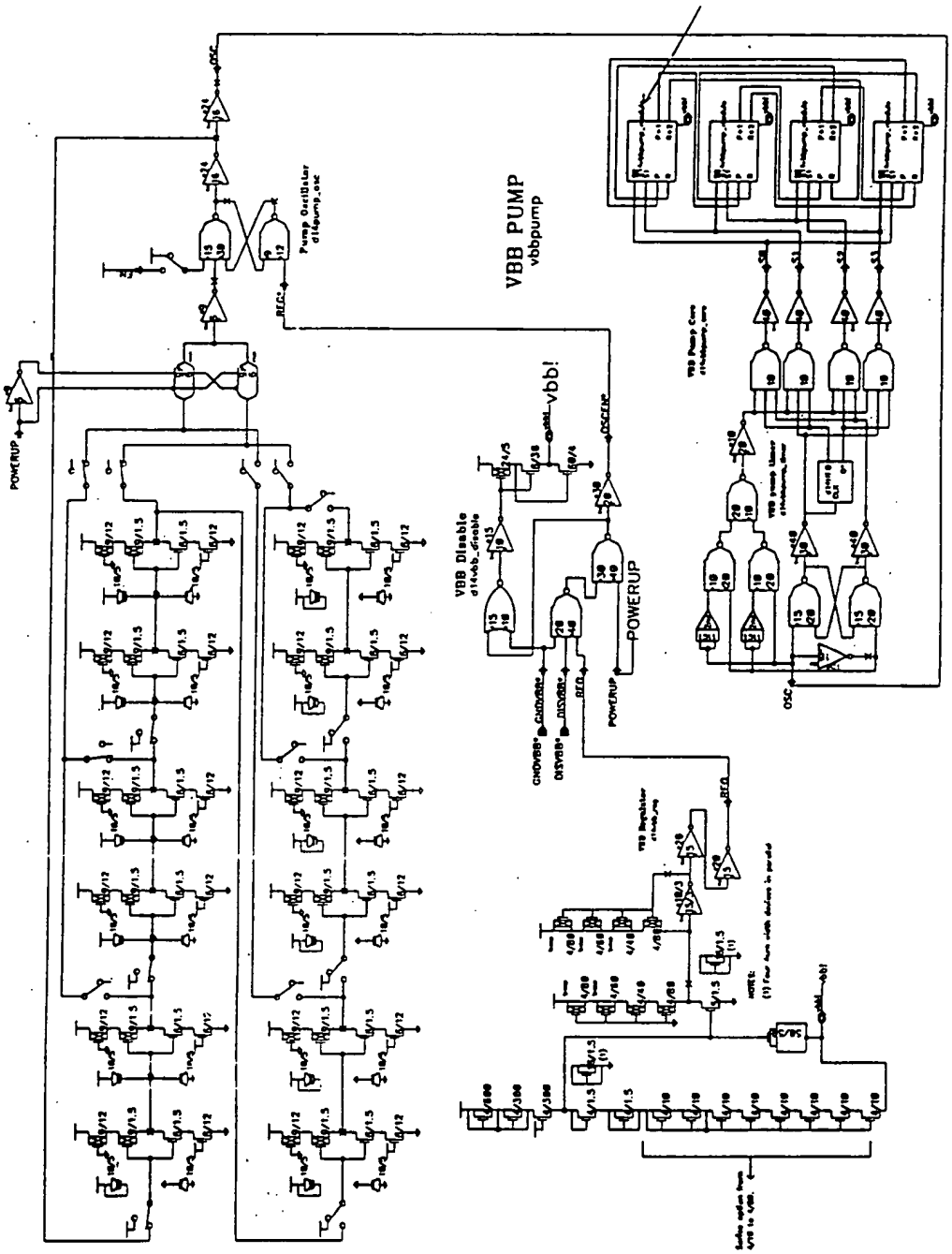


FIGURE 192

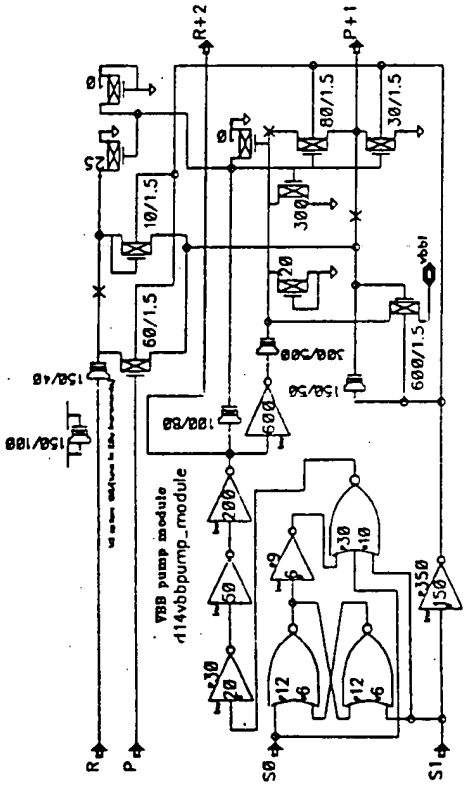

R+2
P+1
0
25
10/1.5
60/1.5
150/40
150/100
80/1.5
30/1.5
300
20
vbb
600/1.5
150/50
100/80
600
200
60
30
20
9
6
30
10
12
6
12
6
350
150
VBB pump module
r114vbbpump_module
R
P
S0
S1

FIGURE 193

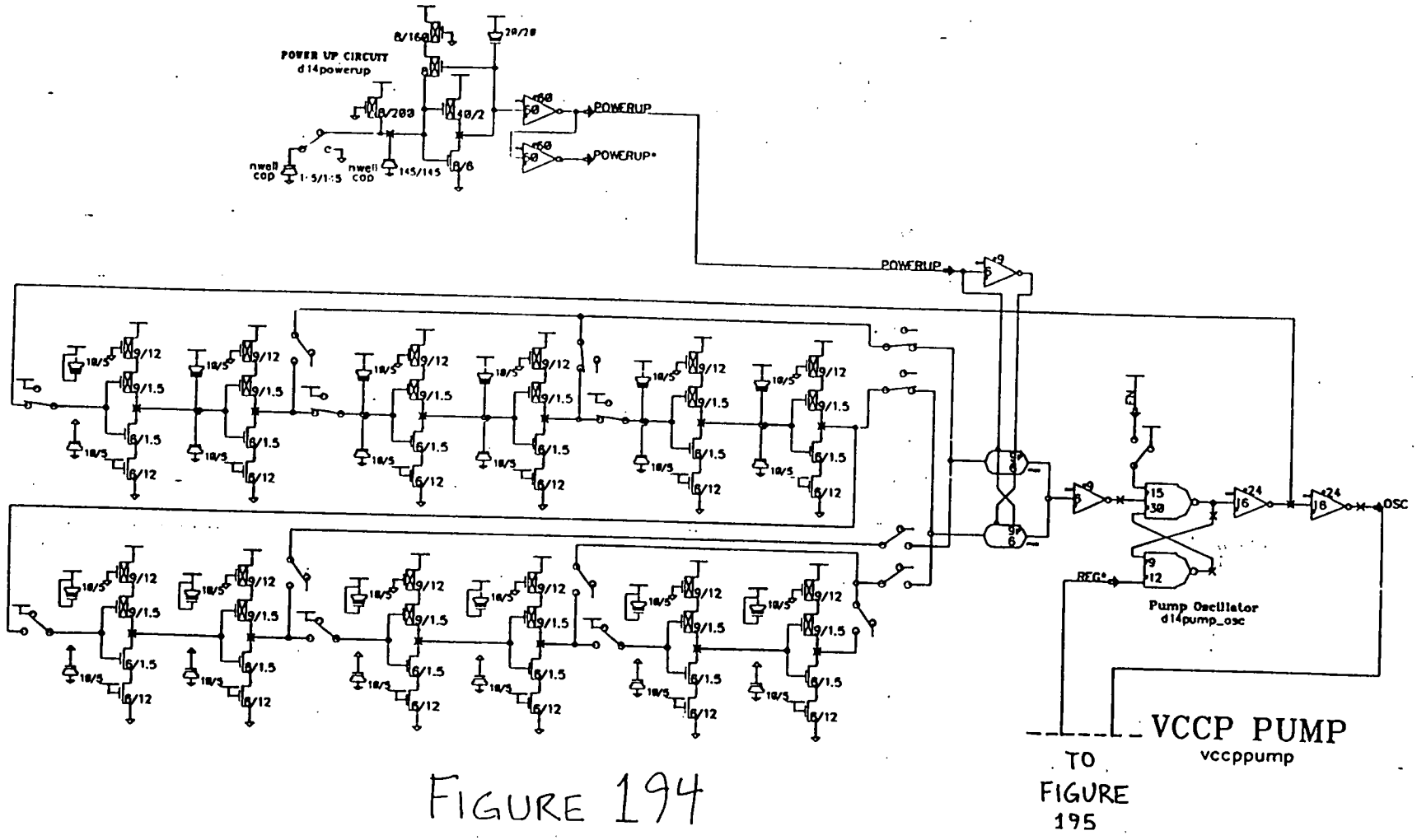

POWER UP CIRCUIT
d14powerup
POWERUP
POWERUP*
nwell cap
nwell COD
Pump Oscillator
d14pump_osc
OSC
REG*
VCCP PUMP
vccppump
TO FIGURE 195

FIGURE 194

FROM FIGURE 194

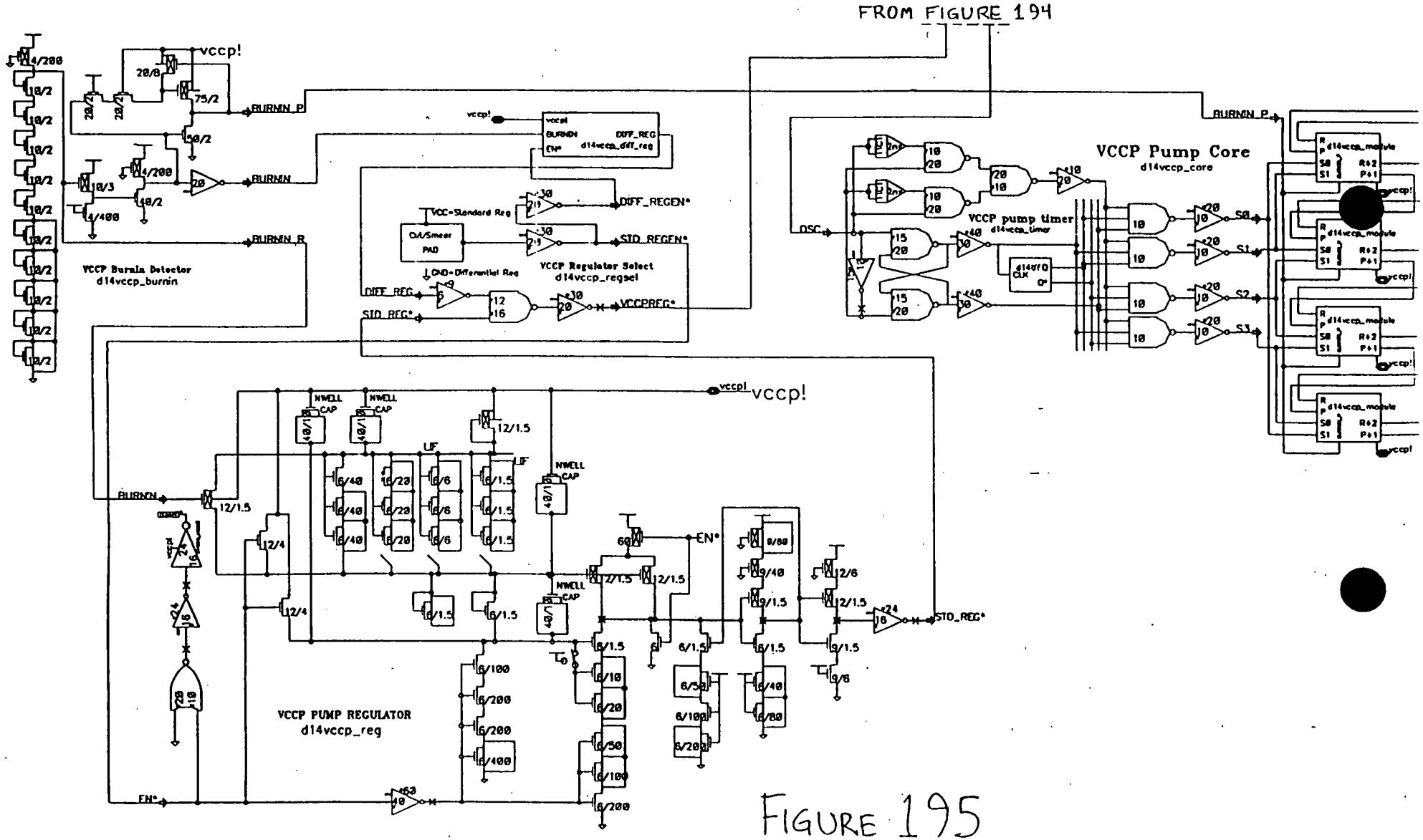


FIGURE 195

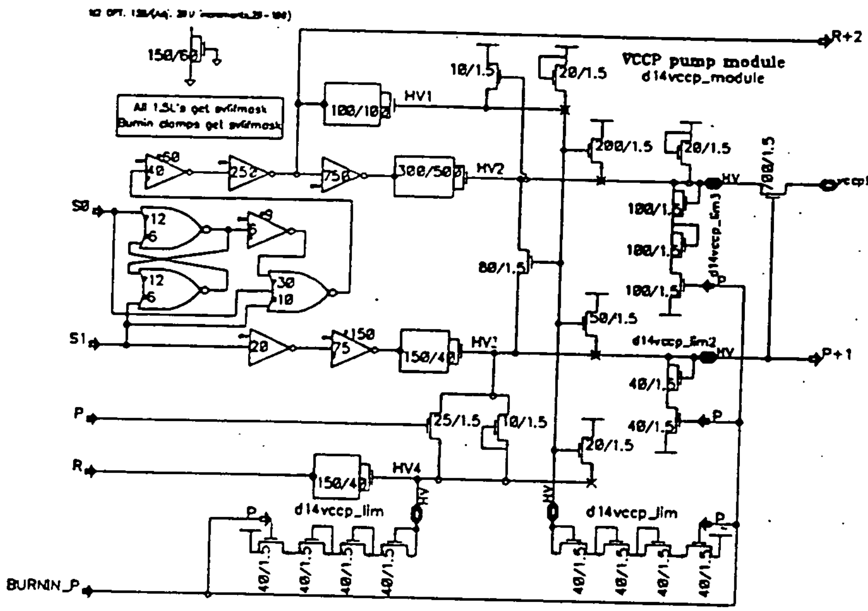

VCCP pump module
d14vccp_module
All 1.5L's get pvt/mask
Burnin clamps get pvt/mask
S0
S1
P
R
BURNIN_P
HV1
HV2
HV4
R+2
P+1
vccp
d14vccp_lim
d14vccp_lim2
d14vccp_lim3

FIGURE 196

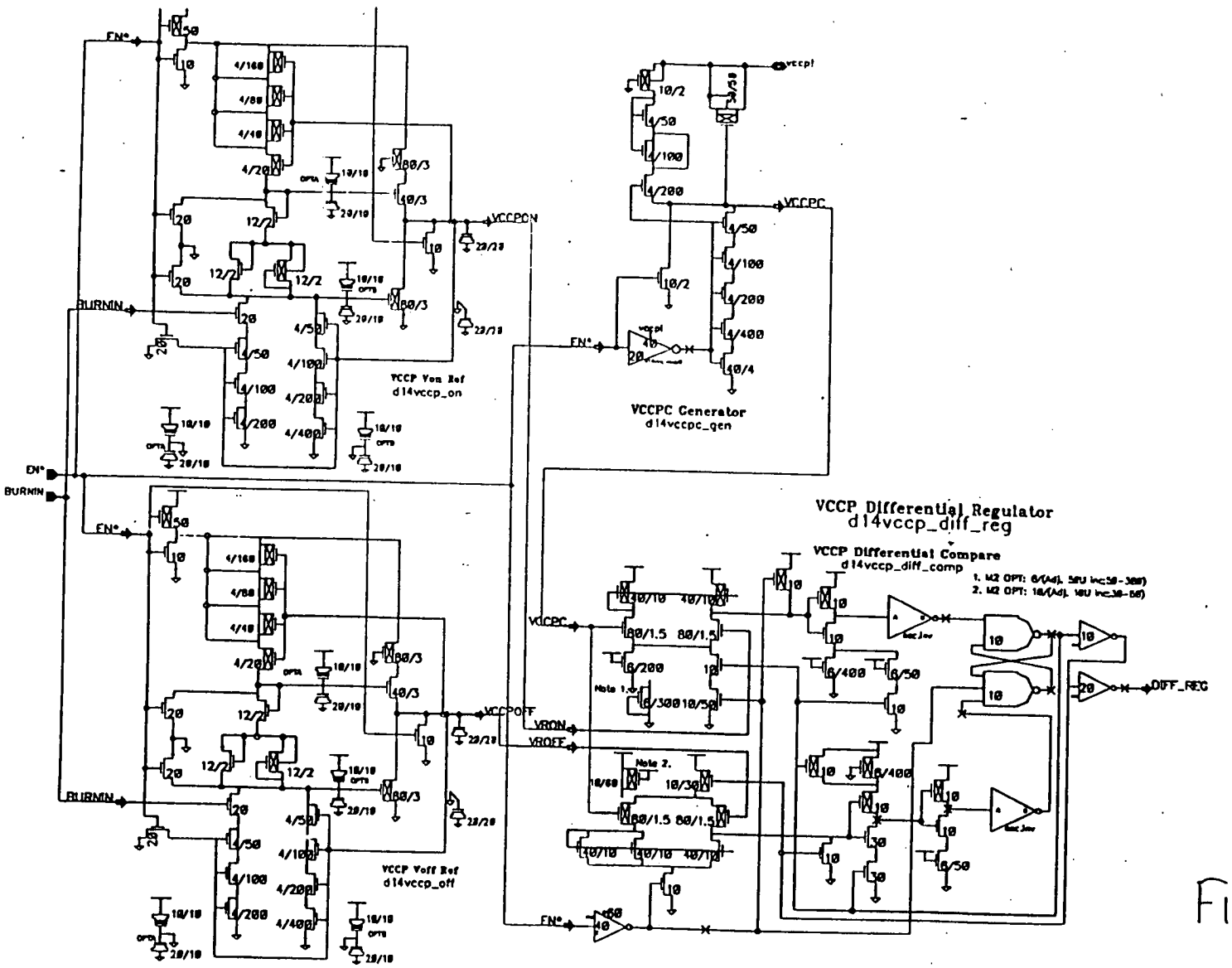

VCCP Von Ref
d14vccp_on
VCCPC Generator
d14vccpc_gen
VCCP Differential Regulator
d14vccp_diff_reg
VCCP Differential Compare
d14vccp_diff_comp
VCCP Voff Ref
d14vccp_off
VCCPON
VCCPC
VCCPOFF
VRON
VROFF
DIFF_REG
BURNIN
EN*

FIGURE 197

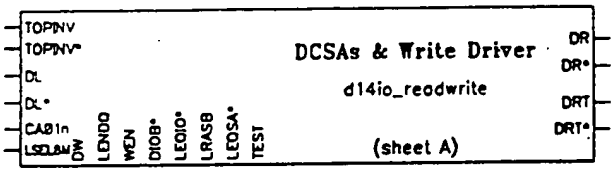


FIGURE 198

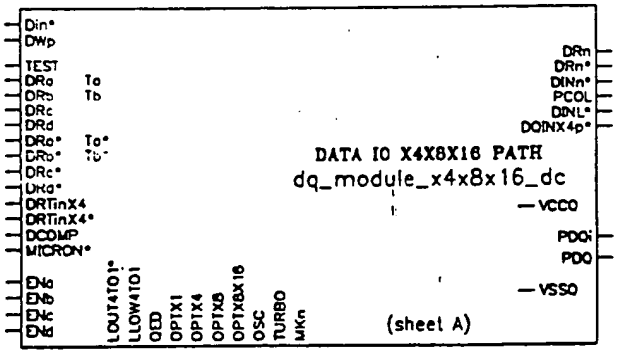


FIGURE 199

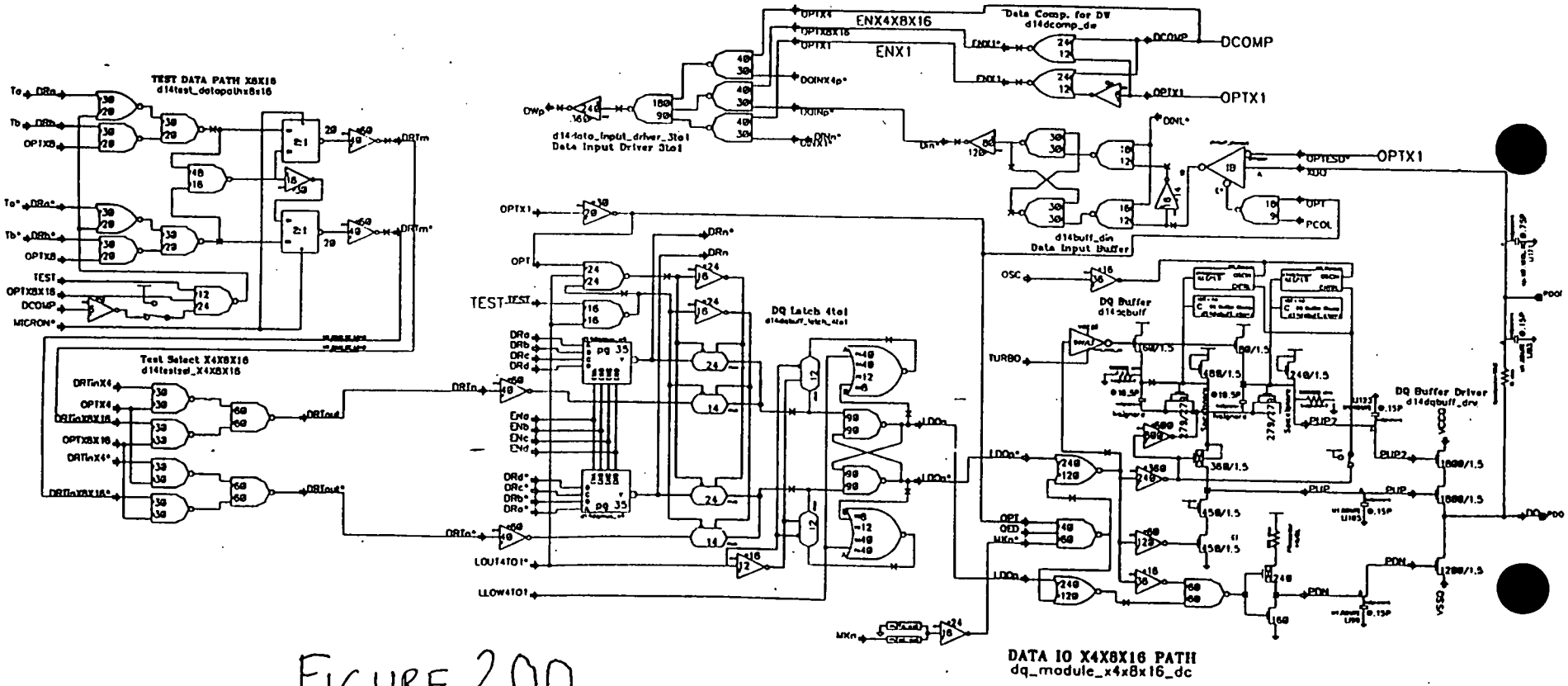

TEST DATA PATH X8X16
d14test_datapathx8x16
Test Select X4X8X16
d14testsel_X4X8X16
ENX4X8X16
ENX1
Data Comp. for DV
d14dcomp_dv
DCOMP
OPTX1
d14data_input_driver_3to1
Data Input Driver 3to1
d14buff_din
Data Input Buffer
DQ Latch 4to1
DQ Buffer
d14dqbuff
DQ Buffer Driver
d14dqbuff_drv
DATA IO X4X8X16 PATH
dq_module_x4x8x16_dc

FIGURE 200

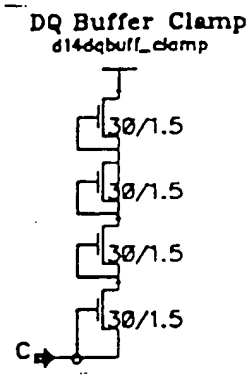


FIGURE 201

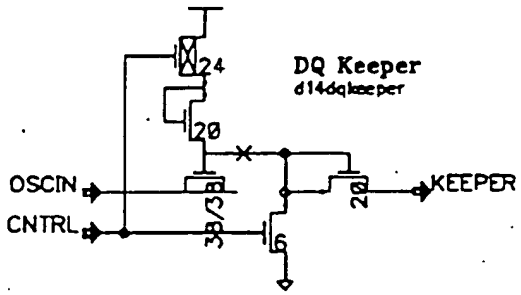


FIGURE 202

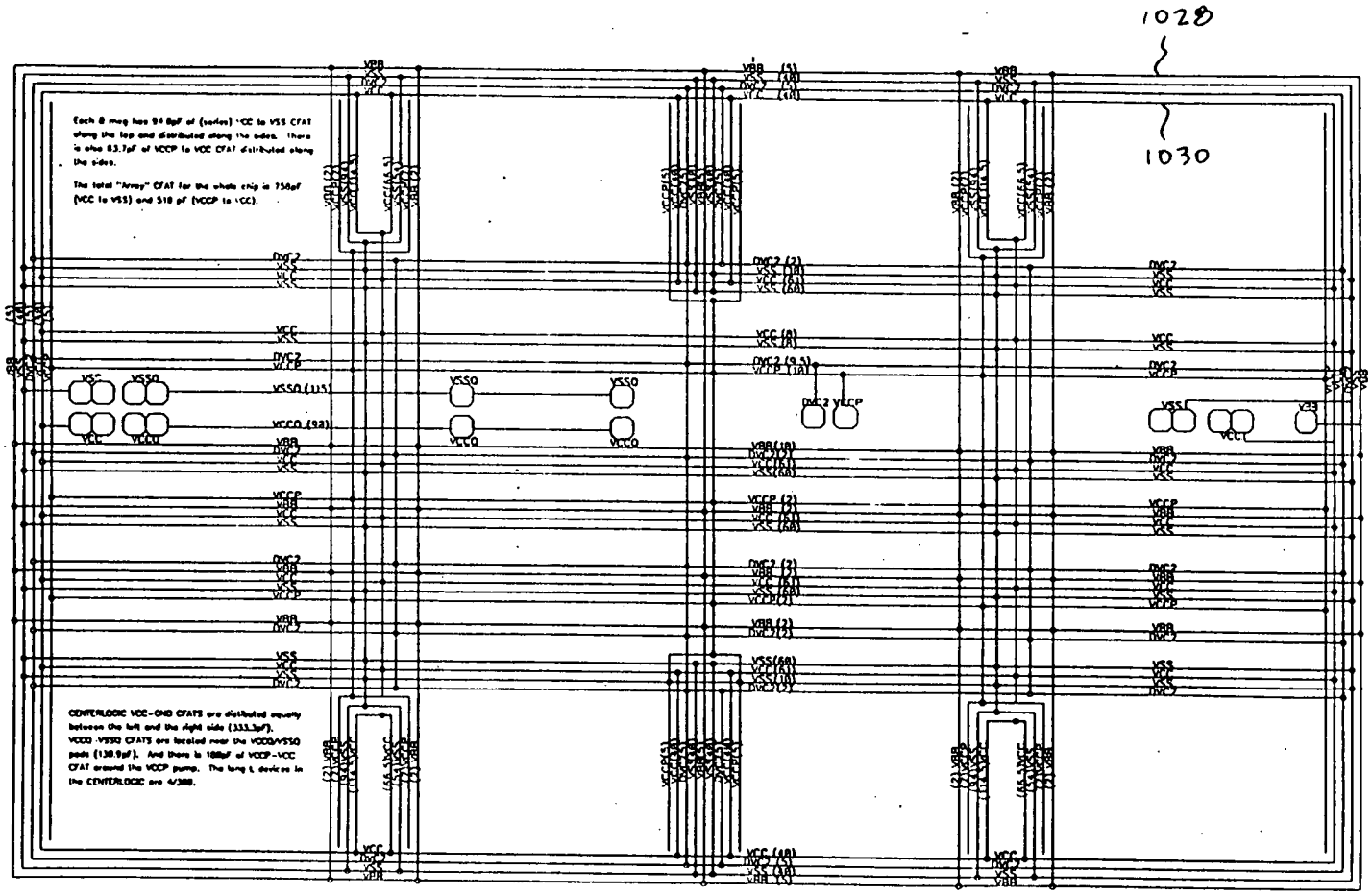


FIGURE 203

CONFIG	ROW ADDRESS		COLUMN ADDRESS	
	8K refresh	4K refresh	8K refresh	4K refresh
4MX16	AØ – A12	AØ – A11	AØ – A8	AØ – A9
8MX8	AØ – A12	AØ – A11	AØ – A9	AØ – A1Ø
16MX4	AØ – A12	–	AØ – A1Ø	AØ – A11
64MX1	AØ – A12	–	AØ – A12	–

FIGURE 204

Test Mode Address Compression (ref to X1) The following column addresses are ignored	
16X	A12, A11, A1Ø, A9
32X	A12, A11, A1Ø, A9, A8 (default customer testmode)
64X	A12, A11, A1Ø, A9, A8, A7
128X	A12, A11, A1Ø, A9, A8, A7, plus row address A12

FIGURE 205

DQ Configuration

(X16)	(X8)	(X4)	(X16)	(X8)	(X4)	(X1)
DQ5	DQ2	DQ0	DQ4	DQ2	DQ0	CA1112<0>
DQ7	DQ3	DQ1	DQ6	DQ3	DQ1	CA1112<1>
DQ13	DQ6	DQ2	DQ12	DQ6	DQ2	CA1112<2>
DQ15	DQ7	DQ3	DQ14	DQ7	DQ3	CA1112<3>
CA910<2>			CA910<3>			
DQ10	DQ5	DQ3	DQ11	DQ5	DQ3	CA1112<3>
DQ8	DQ4	DQ2	DQ9	DQ4	DQ2	CA1112<2>
DQ2	DQ1	DQ1	DQ3	DQ1	DQ1	CA1112<1>
DQ0	DQ0	DQ0	DQ1	DQ0	DQ0	CA1112<0>
CA910<0>			CA910<1>			

FIGURE 206

X8 Configuation

Assembly Pin-out	Schematic Pin-out	Bond Pad PDQ	DW	DR/DR*
DQ1	DQ0	0 1	0 1	0, 1 0, 1
DQ2	DQ1	2 3	2 3	2, 3 2, 3
DQ3	DQ2	4 5	4 5	4, 5 4, 5
DQ4	DQ3	6 7	6 7	6, 7 6, 7
DQ5	DQ4	8 9	8 9	8, 9 8, 9
DQ6	DQ5	10 11	10 11	10, 11 10, 11
DQ7	DQ6	12 13	12 13	12, 13 12, 13
DQ8	DQ7	14 15	14 15	14, 15 14, 15

FIGURE 207

X4 Configuration

Assembly Pin-out	Schematic Pin-out	Bond Pad PDQ	Data Write DW	Data Read DR/DR*
DQ1	DQ0	0	0, 4, 5	0, 1, 4, 5
		1	1	0, 1, 4, 5
DQ2	DQ1	2	2, 6, 7	2, 3, 6, 7
		3	3	2, 3, 6, 7
DQ3	DQ2	12	12	8, 9, 12, 13
		13	13, 8, 9	8, 9, 12, 13
DQ4	DQ3	14	14	10, 11, 14, 15
		15	15, 10, 11	10, 11, 14, 15

X1 Configuration

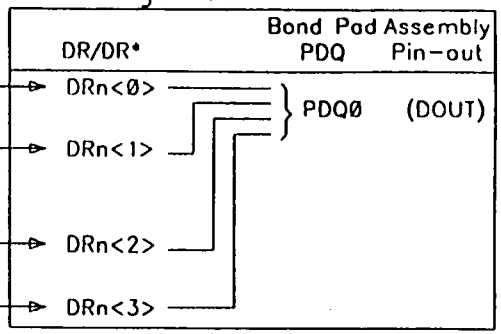


FIGURE 208

DQ Compression

DR/DW	X8 Config PDQ	X8 Config Assembly DQ	X16 Config PDQ	X16 Config Assembly DQ
0,1,4,5	0,1	1	0	1
2,3,6,7	2,3	2	2	3
8,9,12,13	12,13	7	13	14
10,11,14,15	14,15	8	15	16

FIGURE 209

Address Compression

CONFIG	ROW ADDRESS 8K ref	ROW ADDRESS 4K ref	COLUMN ADDRESS 8K ref	COLUMN ADDRESS 4K ref
4MX16	A0 – A12	A0 – A11	A0 – A8	A0 – A9
8MX8	A0 – A12	A0 – A11	A0 – A9	A0 – A10
16MX4	A0 – A12	A0 – A11	A0 – A10	A0 – A11
64MX1	A0 – A12	–	A0 – A12	–

FIGURE 210

Test Mode Address Compression (ref to X1) The following column addresses are ignored	
16X	A12, A11, A10, A9
32X	A12, A11, A10, A9, A8
64X	A12, A11, A10, A9, A8, A7
128X	A12, A11, A10, A9, A8, A7, RA12

FIGURE 211

Cancel Row Fusebank

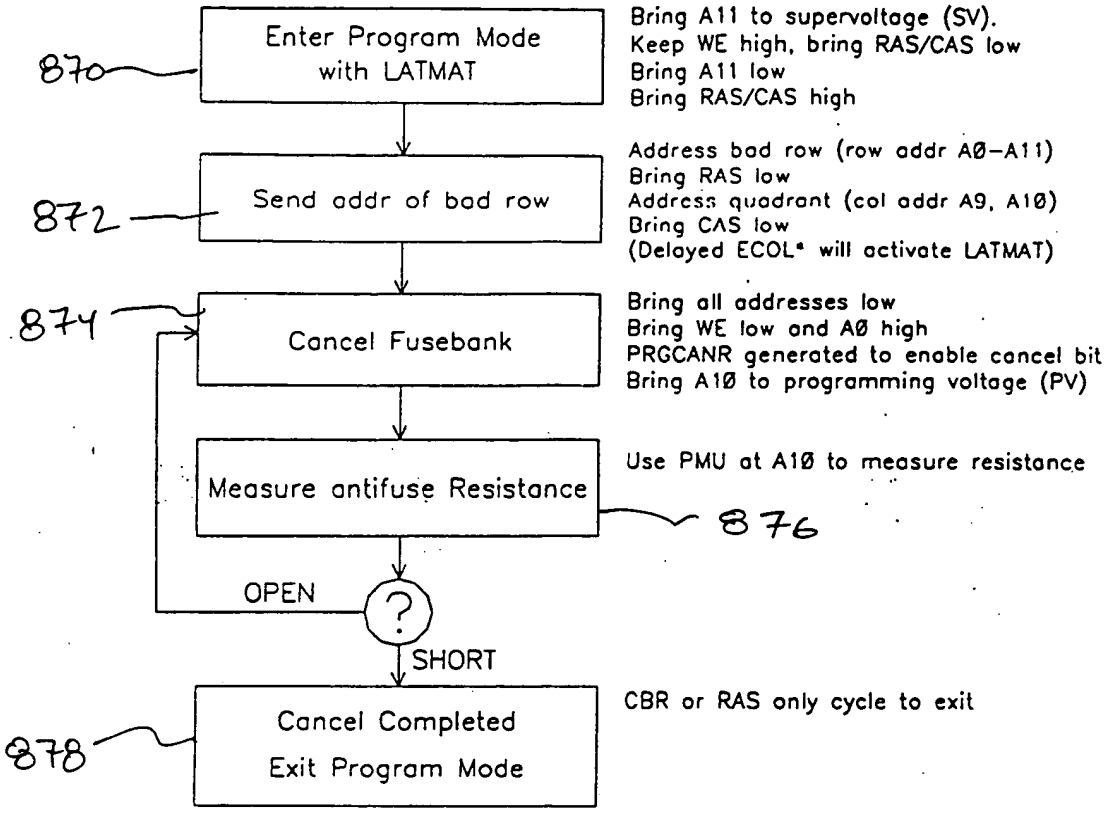


FIGURE 213

Locate Usable Electrical Fusebank and Determine Need for Cancel

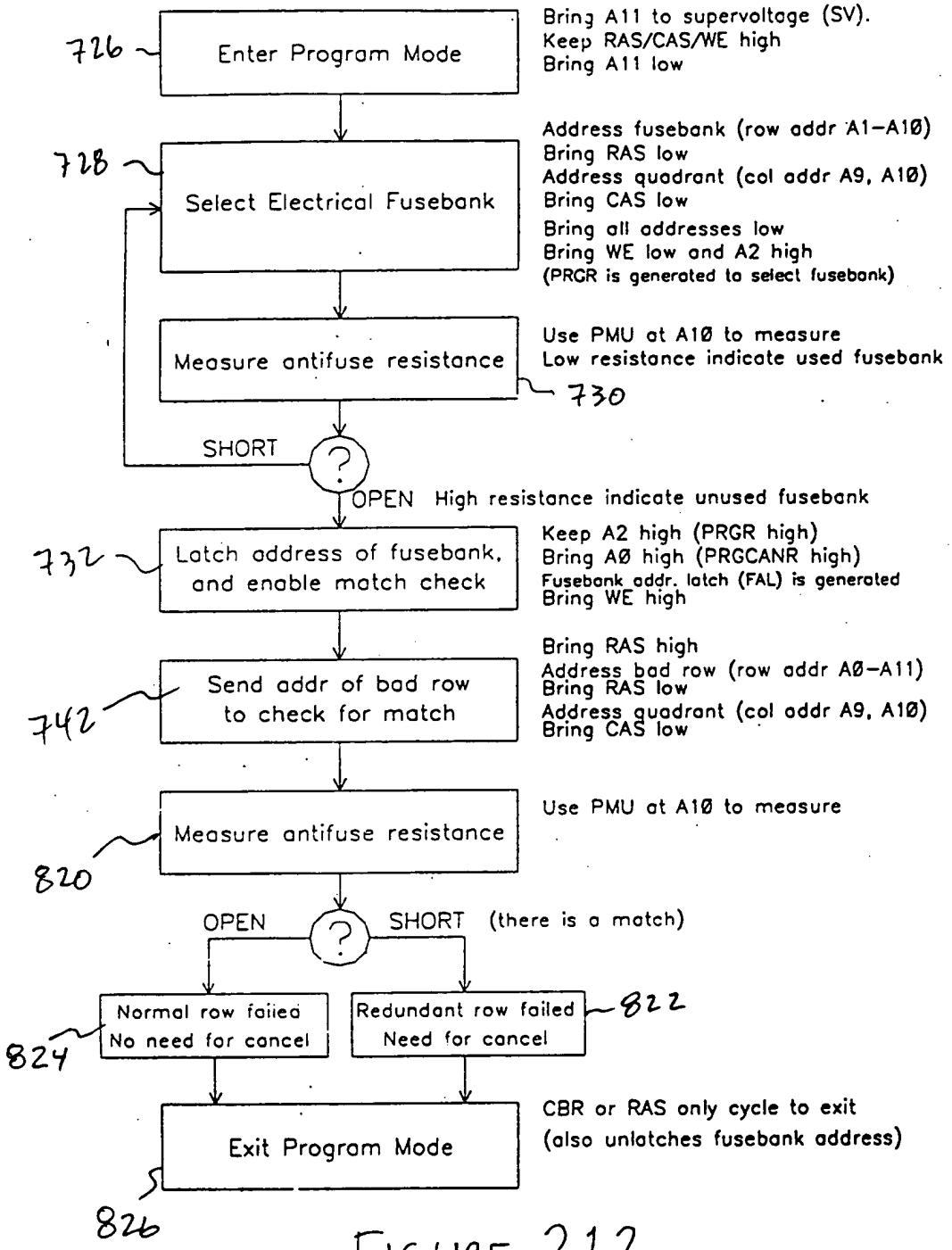


FIGURE 212

Cancel Row Fusebank

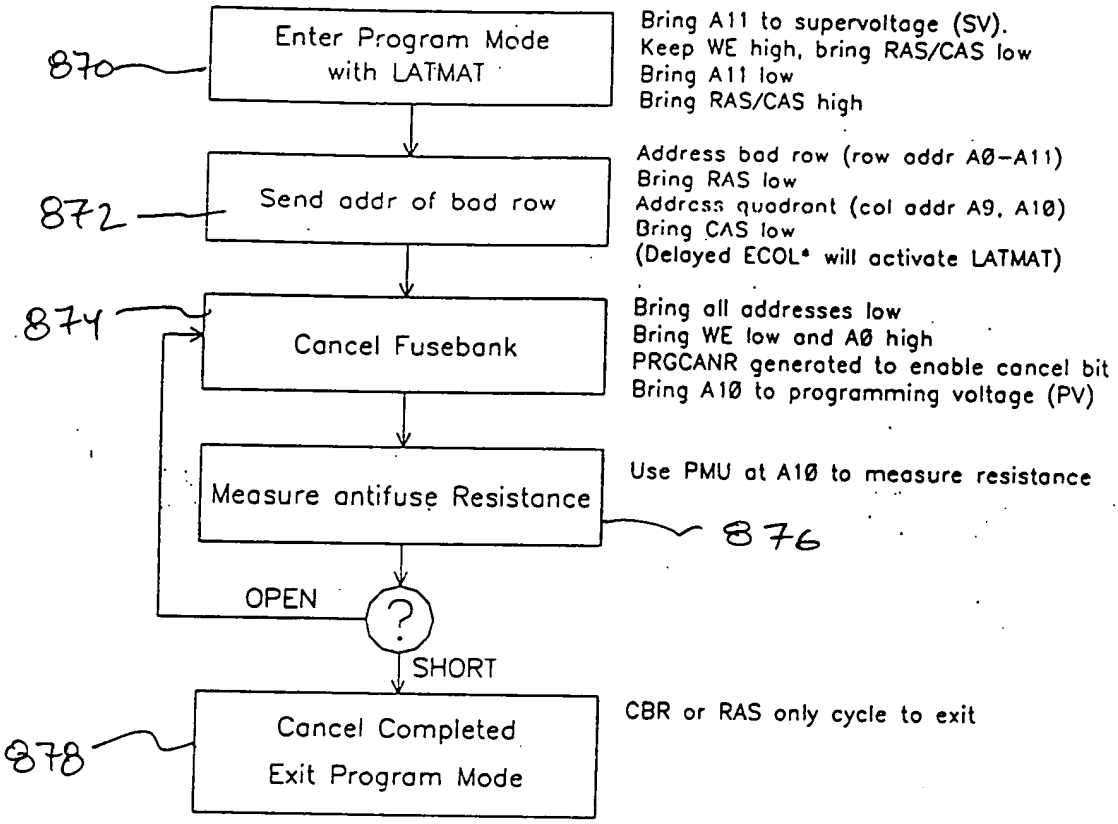


FIGURE 213

Program Row Fusebank

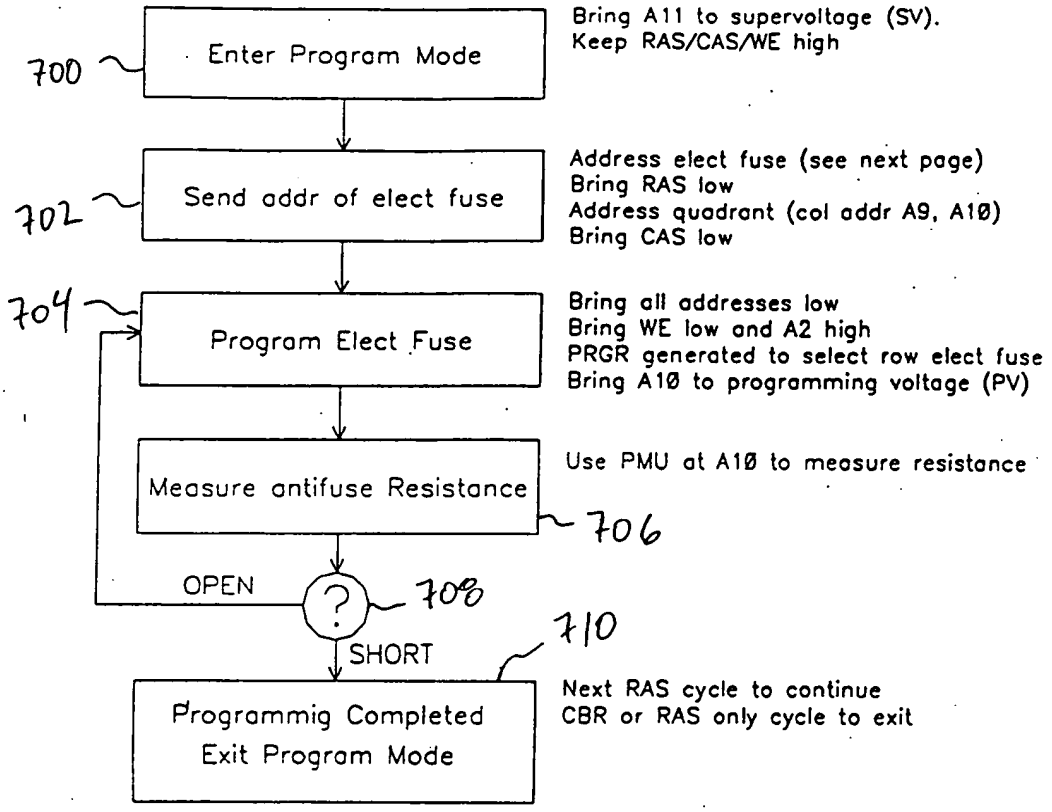


FIGURE 214

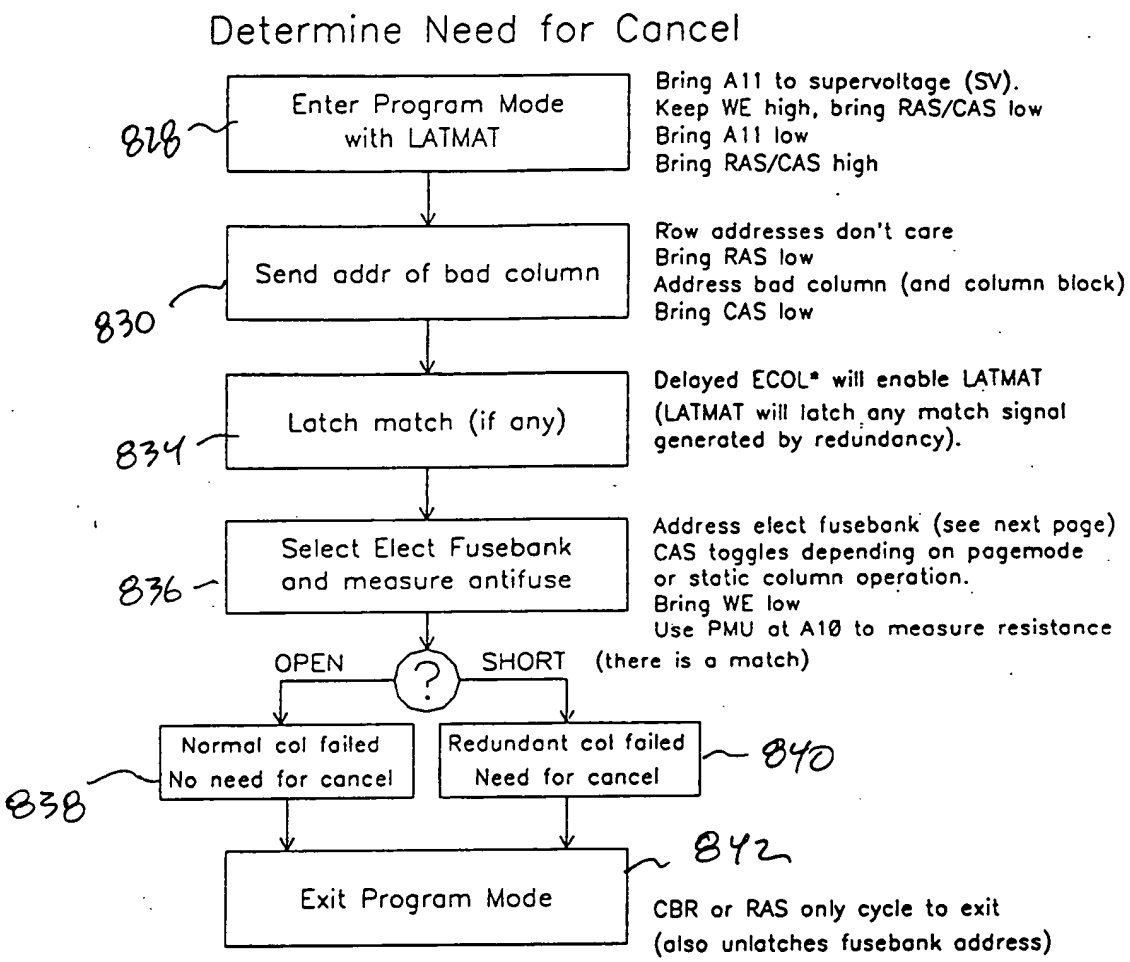

Determine Need for Cancel
Enter Program Mode with LATMAT
828
Bring A11 to supervoltage (SV).
Keep WE high, bring RAS/CAS low
Bring A11 low
Bring RAS/CAS high
Send addr of bad column
830
Row addresses don't care
Bring RAS low
Address bad column (and column block)
Bring CAS low
Latch match (if any)
834
Delayed ECOL* will enable LATMAT
(LATMAT will latch any match signal generated by redundancy).
Select Elect Fusebank and measure antifuse
836
Address elect fusebank (see next page)
CAS toggles depending on pagemode or static column operation.
Bring WE low
Use PMU at A10 to measure resistance
OPEN
?
SHORT
(there is a match)
Normal col failed
No need for cancel
838
Redundant col failed
Need for cancel
840
842
Exit Program Mode
CBR or RAS only cycle to exit
(also unlatches fusebank address)

FIGURE 215

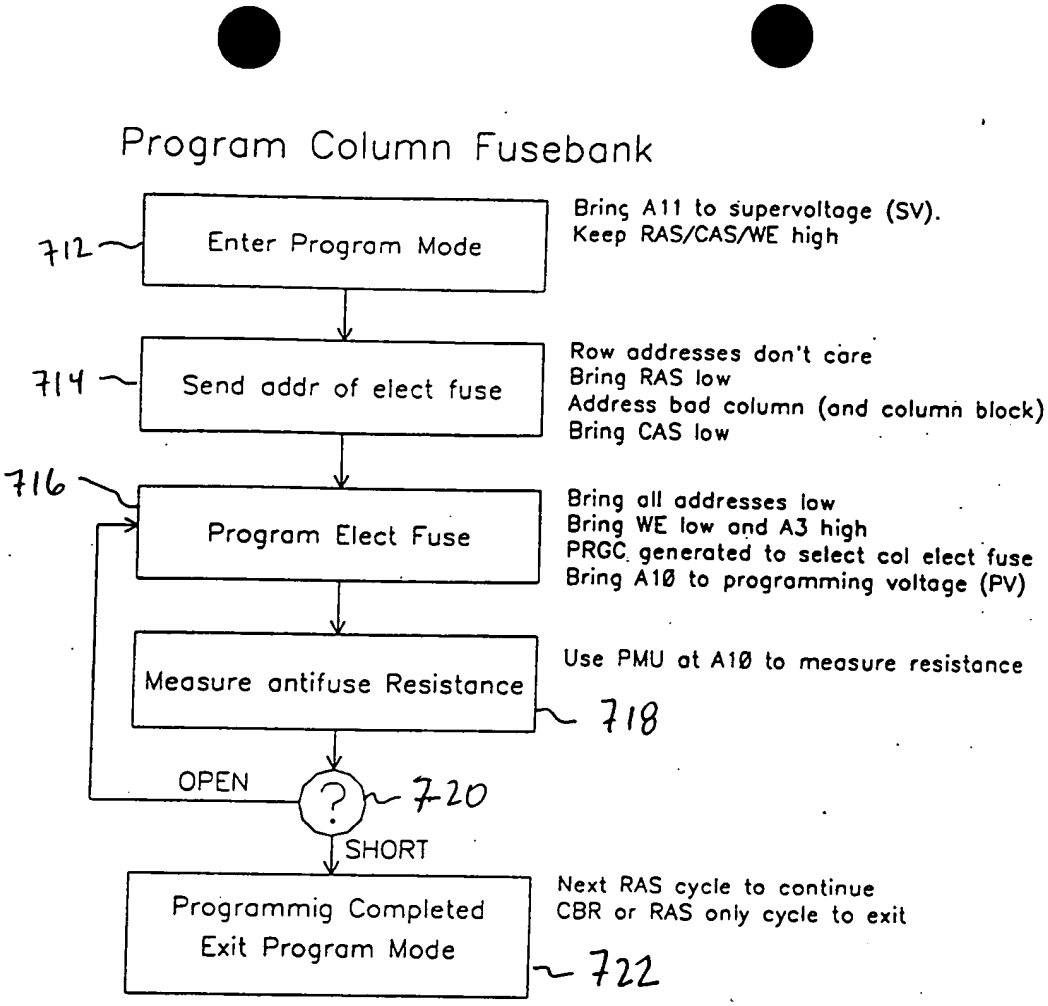

Program Column Fusebank
712
Enter Program Mode
Bring A11 to supervoltage (SV).
Keep RAS/CAS/WE high
714
Send addr of elect fuse
Row addresses don't care
Bring RAS low
Address bad column (and column block)
Bring CAS low
716
Program Elect Fuse
Bring all addresses low
Bring WE low and A3 high
PRGC generated to select col elect fuse
Bring A10 to programming voltage (PV)
Measure antifuse Resistance
Use PMU at A10 to measure resistance
718
OPEN
?
720
SHORT
Programmig Completed
Exit Program Mode
Next RAS cycle to continue
CBR or RAS only cycle to exit
722

FIGURE 216

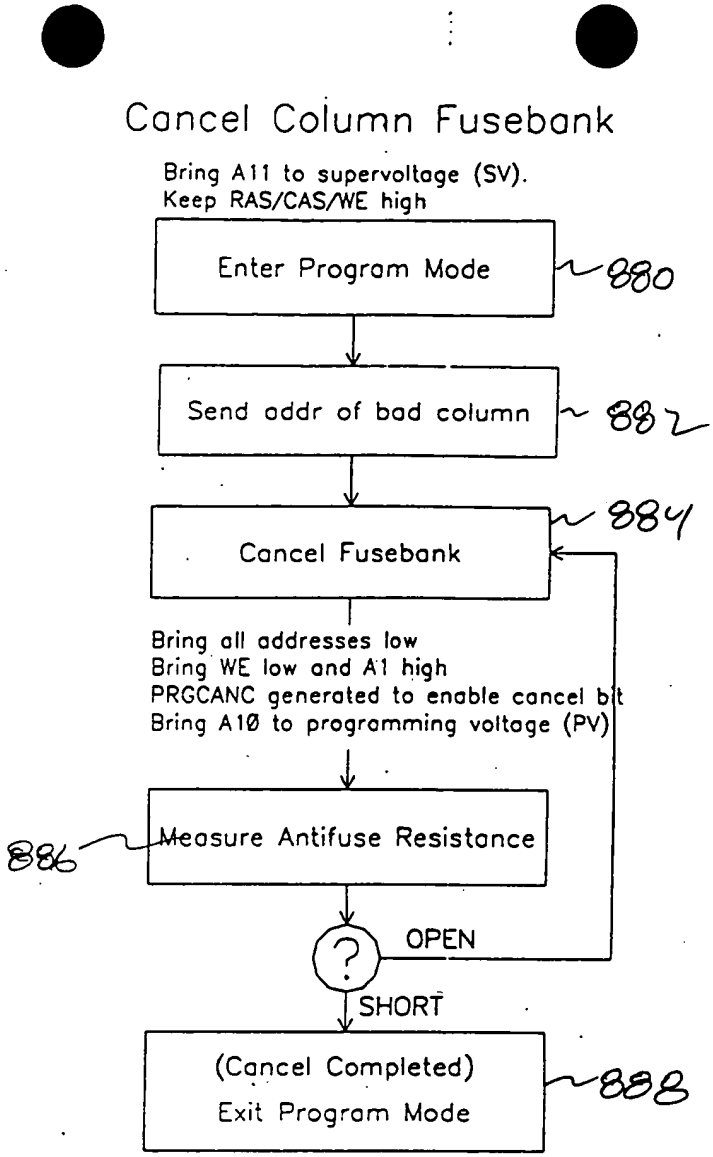

Cancel Column Fusebank
Bring A11 to supervoltage (SV).
Keep RAS/CAS/WE high
Enter Program Mode
880
Send addr of bad column
882
Cancel Fusebank
884
Bring all addresses low
Bring WE low and A1 high
PRGCANC generated to enable cancel bit
Bring A10 to programming voltage (PV)
886
Measure Antifuse Resistance
?
OPEN
SHORT
(Cancel Completed)
Exit Program Mode
888

FIGURE 217

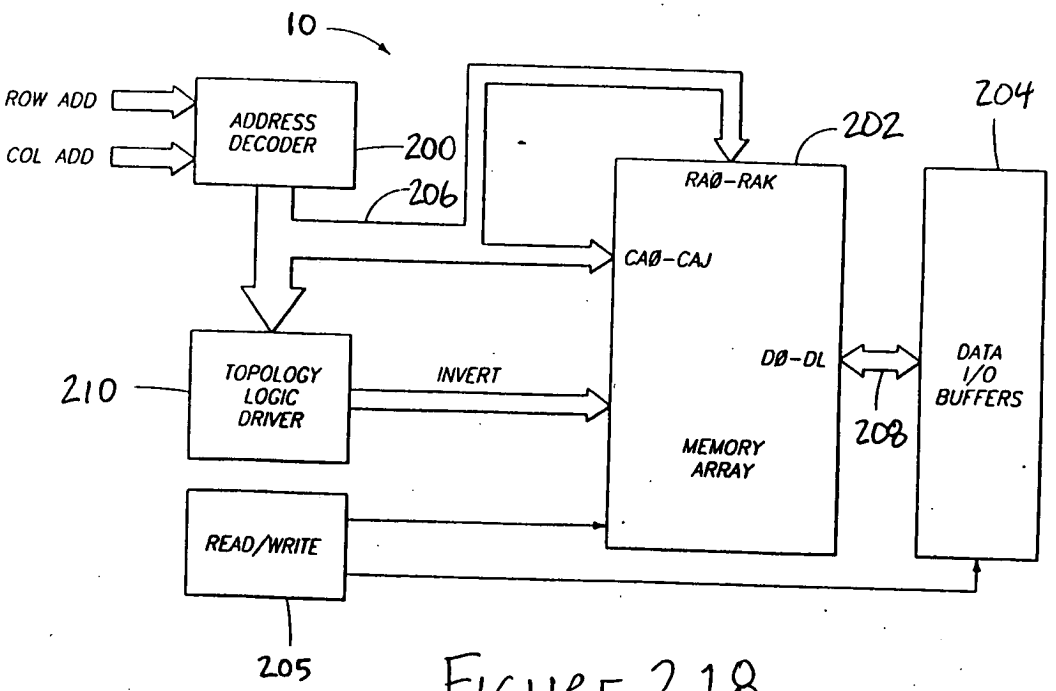

10
ROW ADD
COL ADD
ADDRESS DECODER
200
206
202
204
RA0-RAK
CA0-CAJ
D0-DL
DATA I/O BUFFERS
208
MEMORY ARRAY
210
TOPOLOGY LOGIC DRIVER
INVERT
READ/WRITE
205

FIGURE 218

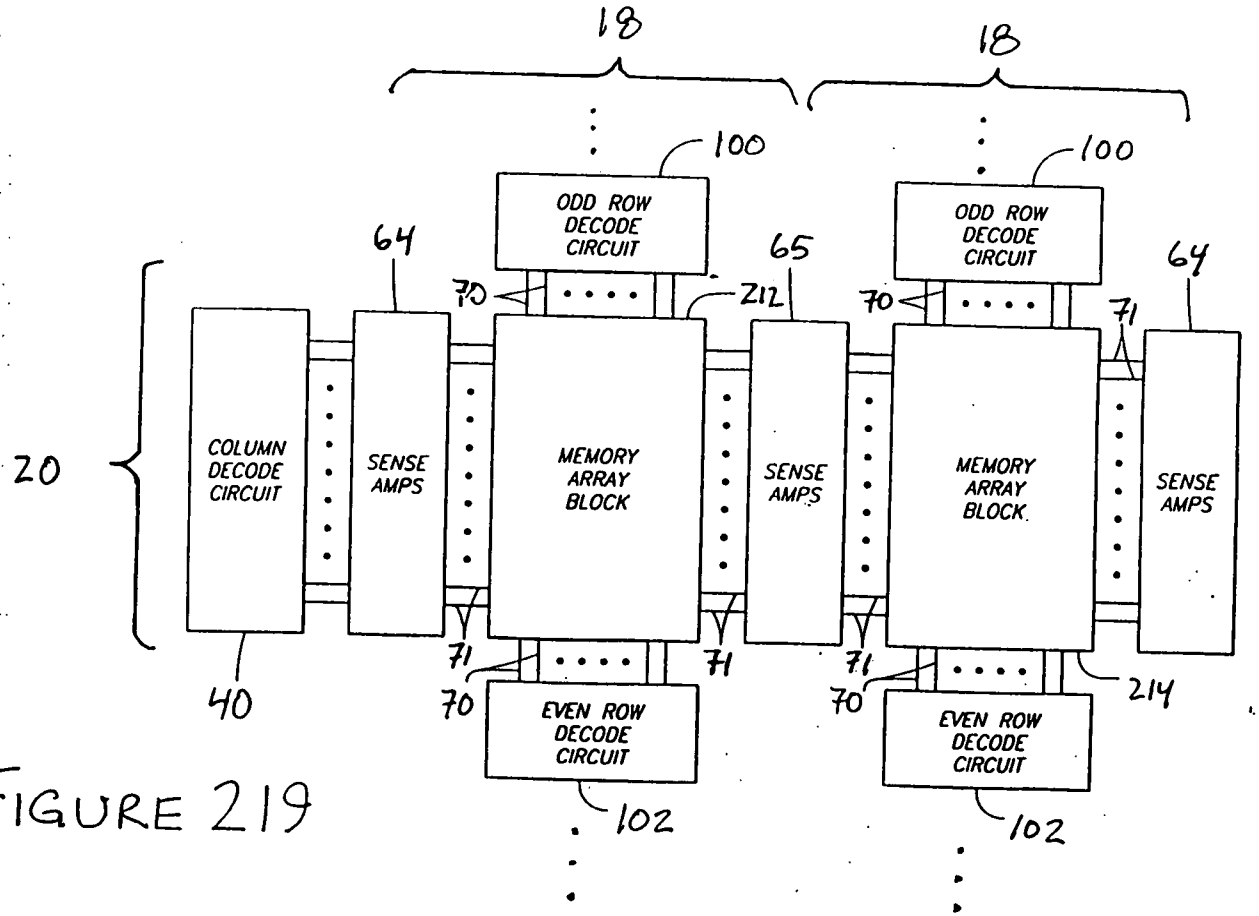

18
18
100
100
ODD ROW DECODE CIRCUIT
ODD ROW DECODE CIRCUIT
64
65
64
70
212
70
71
20
COLUMN DECODE CIRCUIT
SENSE AMPS
MEMORY ARRAY BLOCK
SENSE AMPS
MEMORY ARRAY BLOCK
SENSE AMPS
71
71
71
70
70
214
40
EVEN ROW DECODE CIRCUIT
EVEN ROW DECODE CIRCUIT
102
102

FIGURE 219

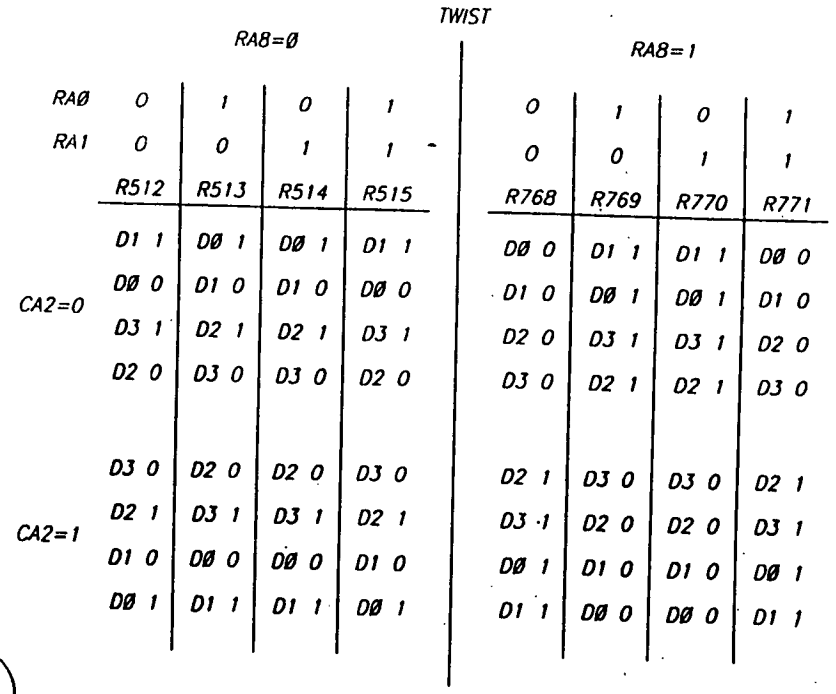


FIGURE 22D

MI28-058

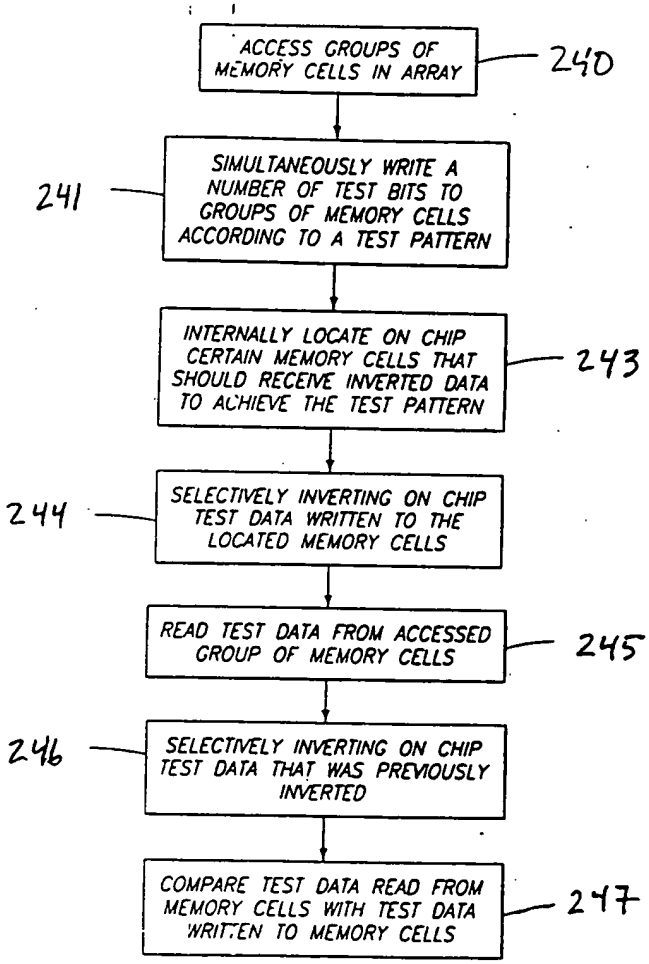

ACCESS GROUPS OF MEMORY CELLS IN ARRAY
240
SIMULTANEOUSLY WRITE A NUMBER OF TEST BITS TO GROUPS OF MEMORY CELLS ACCORDING TO A TEST PATTERN
241
INTERNALLY LOCATE ON CHIP CERTAIN MEMORY CELLS THAT SHOULD RECEIVE INVERTED DATA TO ACHIEVE THE TEST PATTERN
243
SELECTIVELY INVERTING ON CHIP TEST DATA WRITTEN TO THE LOCATED MEMORY CELLS
244
READ TEST DATA FROM ACCESSED GROUP OF MEMORY CELLS
245
SELECTIVELY INVERTING ON CHIP TEST DATA THAT WAS PREVIOUSLY INVERTED
246
COMPARE TEST DATA READ FROM MEMORY CELLS WITH TEST DATA WRITTEN TO MEMORY CELLS
247

FIGURE 221

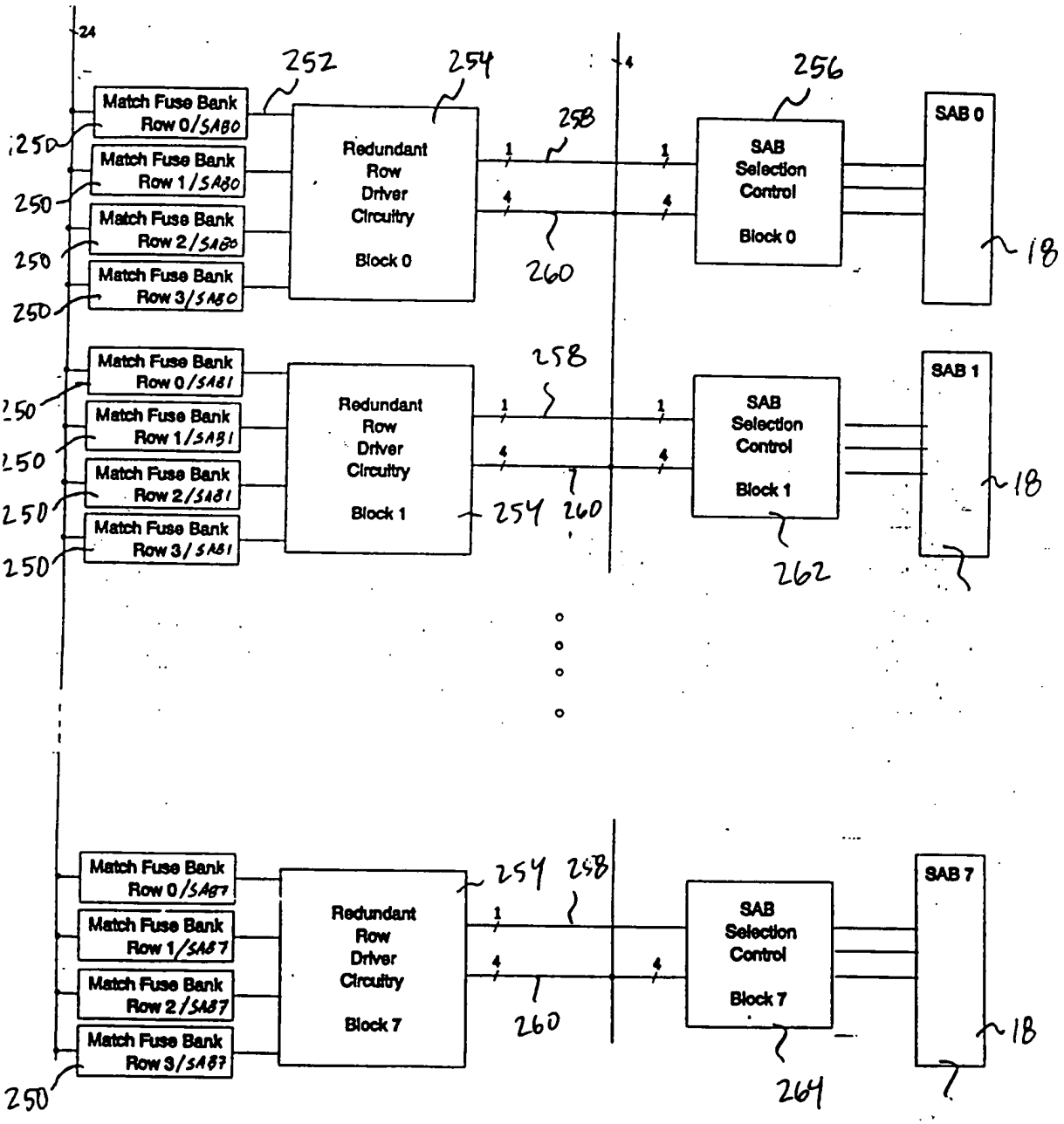

24
252
254
256
Match Fuse Bank Row 0/SAB0
Match Fuse Bank Row 1/SAB0
Match Fuse Bank Row 2/SAB0
Match Fuse Bank Row 3/SAB0
250
Redundant Row Driver Circuitry Block 0
258
260
SAB Selection Control Block 0
SAB 0
18
Match Fuse Bank Row 0/SAB1
Match Fuse Bank Row 1/SAB1
Match Fuse Bank Row 2/SAB1
Match Fuse Bank Row 3/SAB1
Redundant Row Driver Circuitry Block 1
SAB Selection Control Block 1
SAB 1
262
Match Fuse Bank Row 0/SAB7
Match Fuse Bank Row 1/SAB7
Match Fuse Bank Row 2/SAB7
Match Fuse Bank Row 3/SAB7
Redundant Row Driver Circuitry Block 7
SAB Selection Control Block 7
SAB 7
264

FIGURE 22

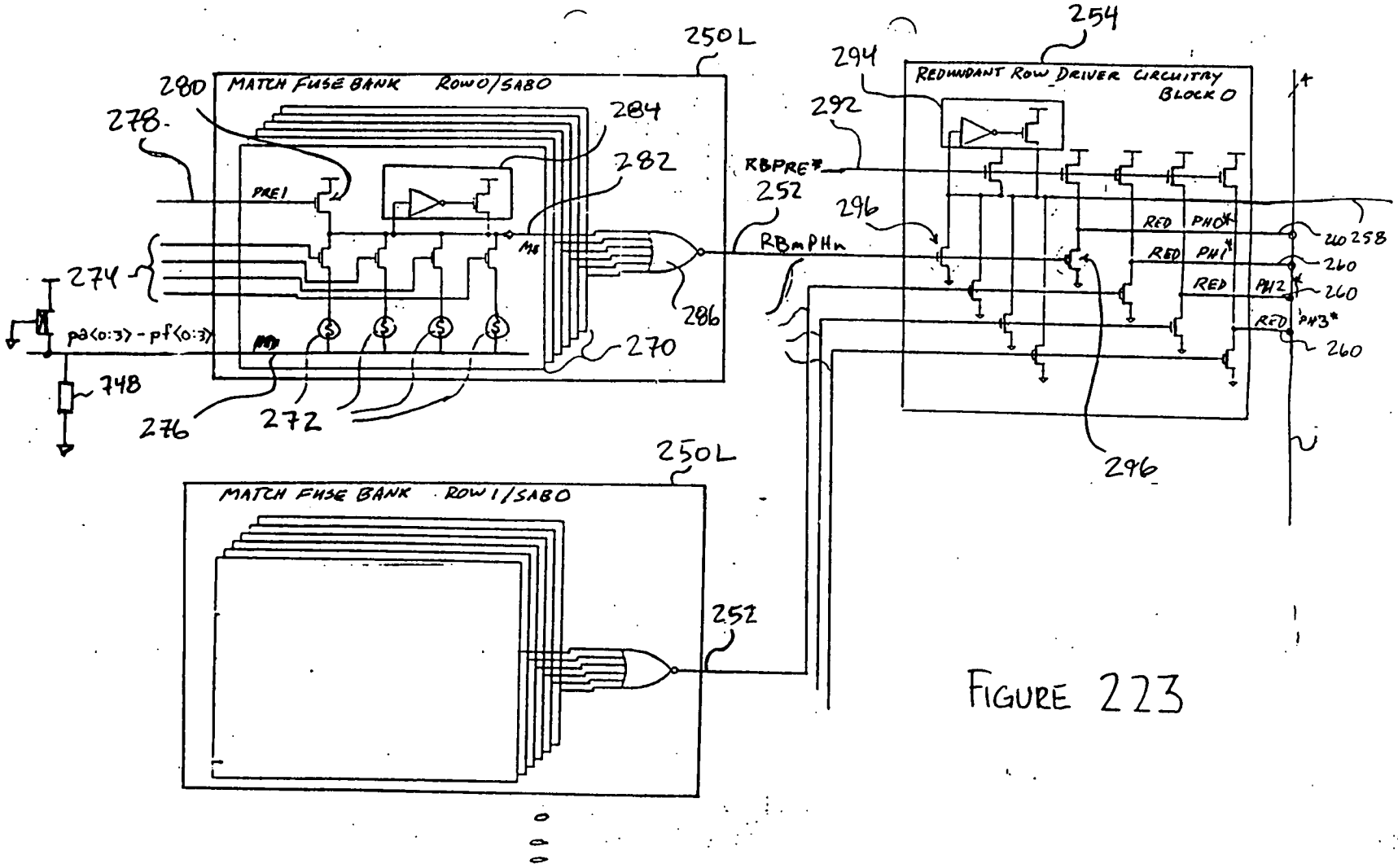

250L
MATCH FUSE BANK ROW 0/SABO
280
278
284
282
PRE1
274
pa<0:3> - pf<0:3>
M6
286
270
748
276
272
252
RBPRE*
RBmPHn
254
294
292
296
REDUNDANT ROW DRIVER CIRCUITRY BLOCK 0
RED PH0*
RED PH1*
RED PH2*
RED PH3*
258
260
250L
MATCH FUSE BANK ROW 1/SABO
252

FIGURE 223

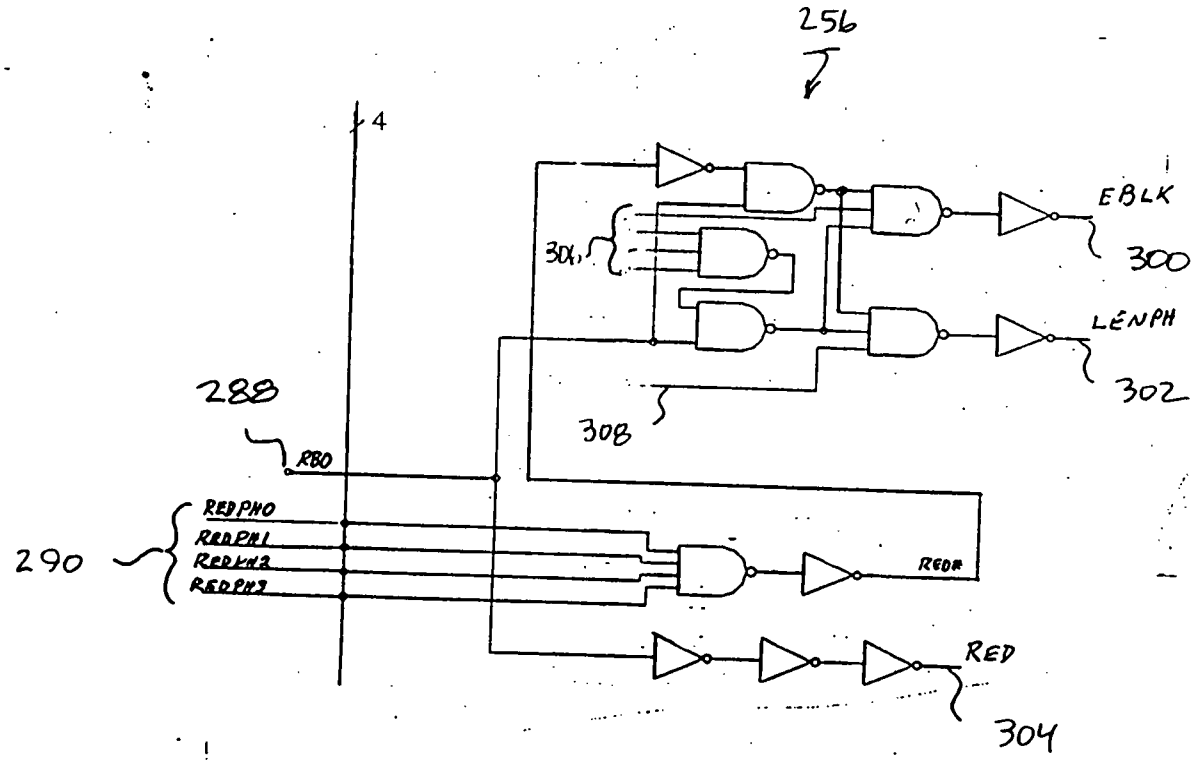

256
4
EBLK
300
LENPH
302
301
308
288
RBO
290
REDPH0
REDPH1
REDPH2
REDPH3
RED#
RED
304

FIGURE 224

SAB0								
OPERATION TYPE			SELECTION CONTROL					
			Input			Output		
Primary Row to Fire ?	Redundant Row In SAB0 ?	Primary Address In SAB0 ?	Primary Address Lines	One of $\overline{REDPH0}$-$\overline{REDPR3}$	$\overline{RB0}$	EBLK	LENPH	RED
yes	[redacted]	yes	1	1	1	1	1	0
		no	0	1	1	0	0	0
no	yes	yes	1	0	0	1	1	1
		no	0	0	0	1	1	1
	no	yes	1	0	1	0	0	0
		no	0	0 or 1*	1	0	0	0

*Depending on whether redundant row in another SAB is to fire

FIGURE 225

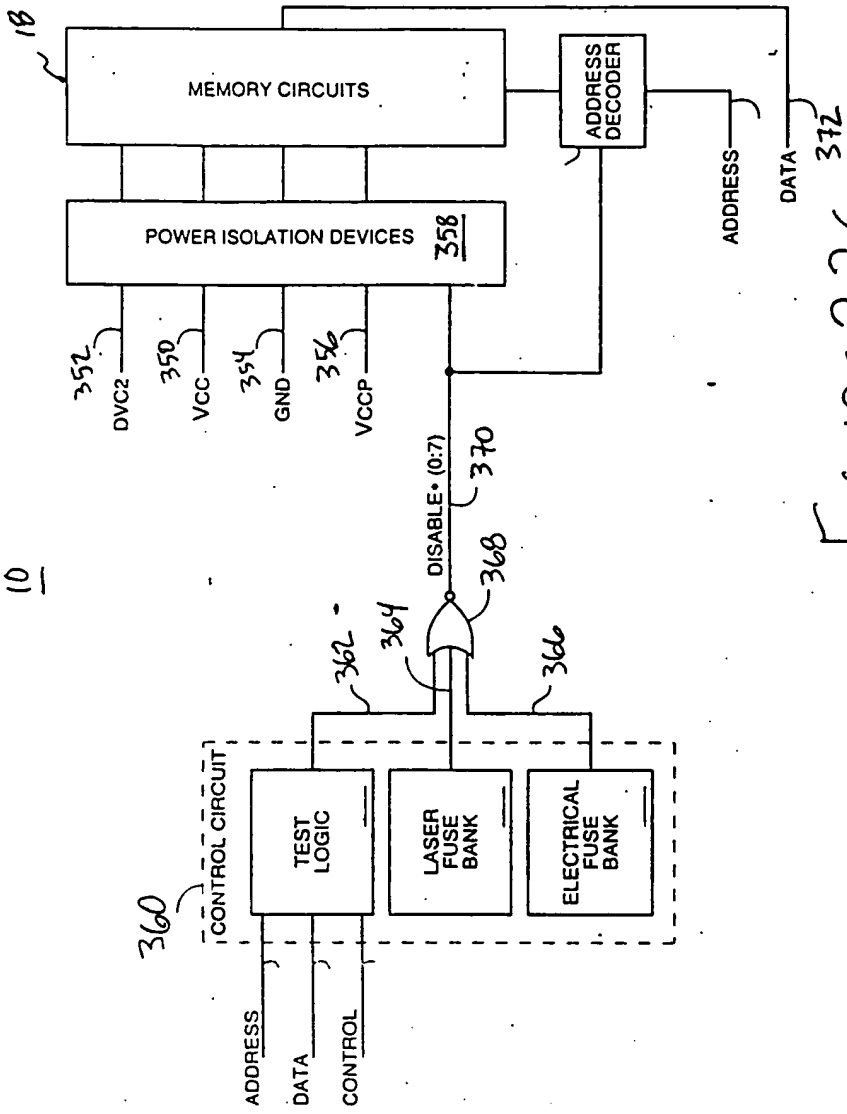

18
MEMORY CIRCUITS
ADDRESS DECODER
ADDRESS
DATA
372
POWER ISOLATION DEVICES
358
352
DVC2
350
VCC
354
GND
356
VCCP
DISABLE• (0:7)
370
368
362
364
366
10
CONTROL CIRCUIT
360
TEST LOGIC
LASER FUSE BANK
ELECTRICAL FUSE BANK
ADDRESS
DATA
CONTROL

FIGURE 226

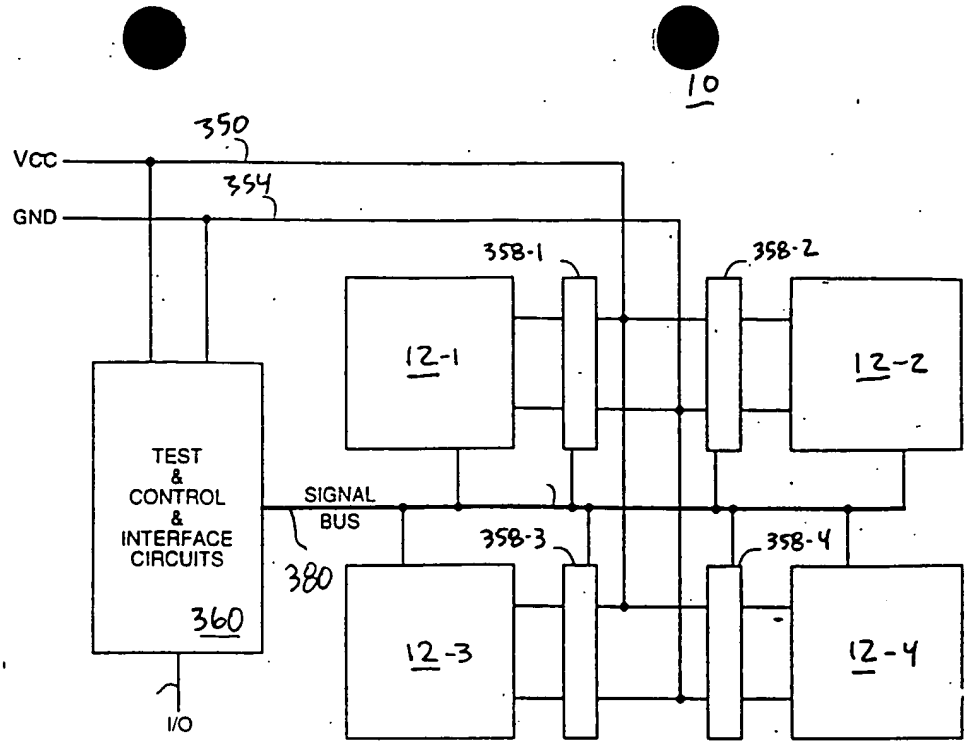


FIGURE 227

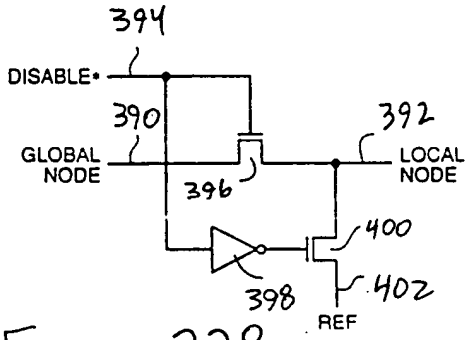


FIGURE 228

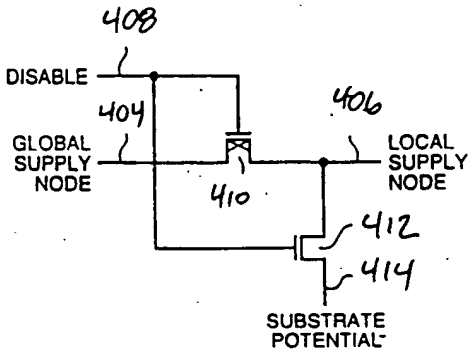


FIGURE 229

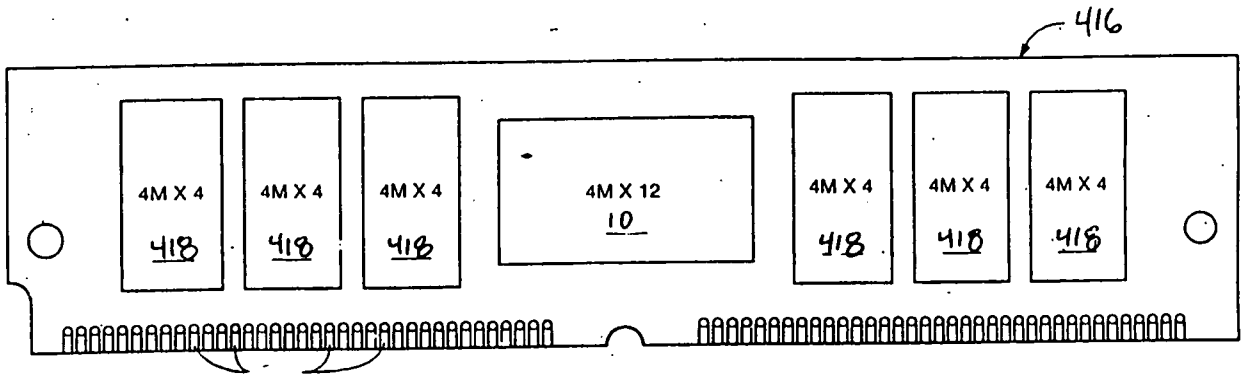

416
4M X 4
418
4M X 4
418
4M X 4
418
4M X 12
10
4M X 4
418
4M X 4
418
4M X 4
418

FIGURE 230

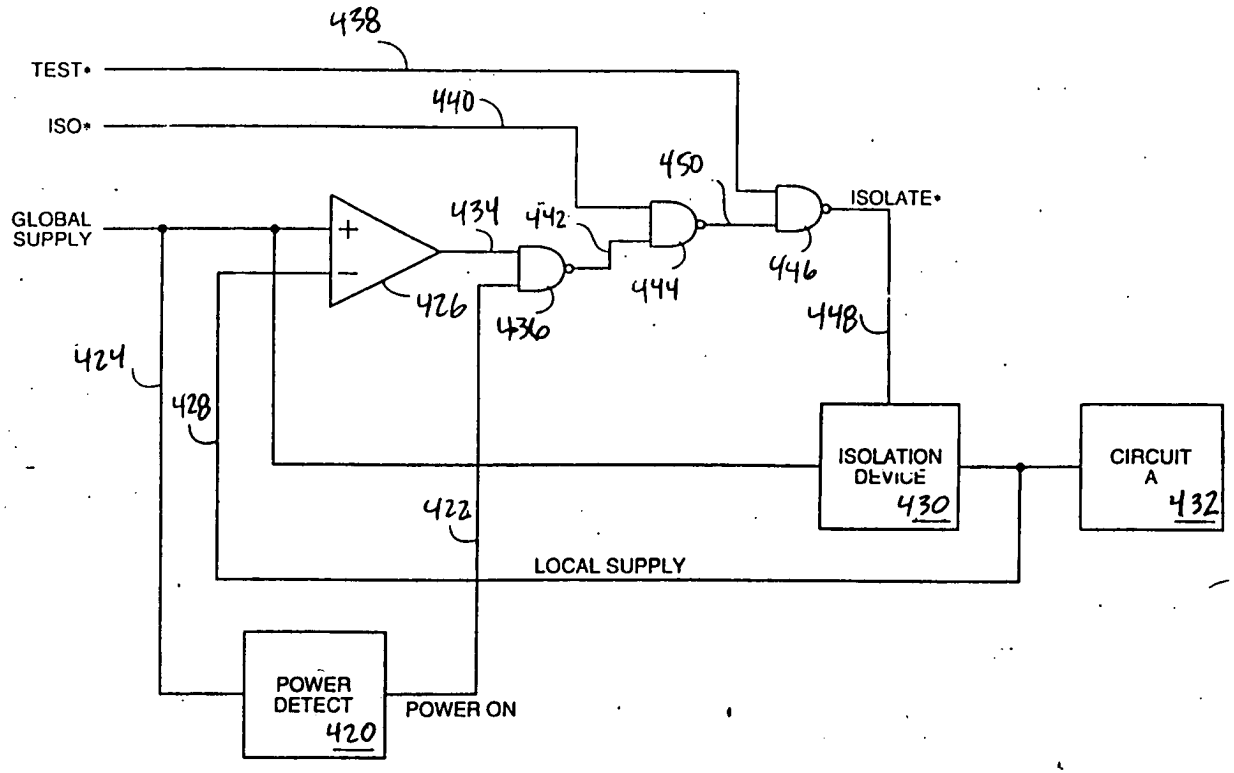

438
TEST*
440
ISO*
450
ISOLATE*
GLOBAL SUPPLY
434
442
426
444
446
436
448
424
428
ISOLATION DEVICE 430
CIRCUIT A 432
422
LOCAL SUPPLY
POWER DETECT 420
POWER ON

FIGURE 231

Anti-fuse not blown, Address=Ø
Anti-fuse blown, Address=1

Row Antifuse Selection Within Each Bank

Fuse Selection Address				Repair Address=1
A4	A3	A2	A1	
Ø	Ø	Ø	Ø	A1
Ø	Ø	Ø	1	A2
Ø	Ø	1	Ø	A3
Ø	Ø	1	1	A4
Ø	1	Ø	Ø	A5
Ø	1	Ø	1	A6
Ø	1	1	Ø	A7
Ø	1	1	1	A8
1	Ø	Ø	Ø	A9
1	Ø	Ø	1	A1Ø
1	Ø	1	Ø	AØ
1	Ø	1	1	A11
1	1	Ø	Ø	Enable Bank
1	1	Ø	1	—
1	1	1	Ø	—
1	1	1	1	—

FIGURE 232

Row Fusebank Enable Selection

Row Fusebank	Fusebank Selection Address A10 A9	A8	A7	A6	A5
RØ		Ø	Ø	Ø	Ø
R1		Ø	Ø	Ø	1
R2		Ø	Ø	1	Ø
R3		Ø	Ø	1	1
R4		Ø	1	Ø	Ø
R5		Ø	1	Ø	1
R6		Ø	1	1	Ø
R7		Ø	1	1	1
R8		1	Ø	Ø	Ø
R9		1	Ø	Ø	1
R10		1	Ø	1	Ø
R11		1	Ø	1	1
R12		1	1	Ø	Ø
R13		1	1	Ø	1
R14		1	1	1	Ø
R15		1	1	1	1
LEFT	Ø Ø				
RIGHT	Ø 1				

FIGURE 233

Column Antifuse Selection Within Each Bank

Fuse Selection Address			Repair Address=1
A1	A0	A6	
0	0	1	A2
0	0	0	A3
0	1	1	A4
0	1	0	A5
1	0	1	A6
1	0	0	A7
1	1	0	A8
1	1	1	BANK ENABLE

FIGURE 234

Column Fusebank Enable Selection

Column Fusebank	Fusebank Selection Address A10	A9	A8	A7
CØ	Ø	Ø	Ø	Ø
C1	Ø	Ø	Ø	1
C2	Ø	Ø	1	Ø
C3	Ø	Ø	1	1
C4	Ø	1	Ø	Ø
C5	Ø	1	Ø	1
C6	Ø	1	1	Ø
C7	Ø	1	1	1
C8	1	Ø	Ø	Ø
C9	1	Ø	Ø	1
C1Ø	1	Ø	1	Ø
C11	1	Ø	1	1
C12	1	1	Ø	Ø
C13	1	1	Ø	1
C14	1	1	1	Ø
C15	1	1	1	1

FIGURE 235

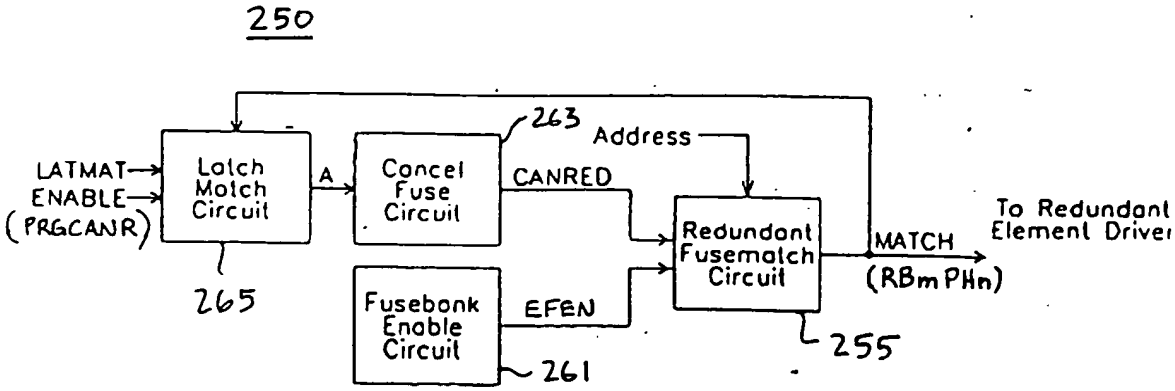

250
LATMAT
ENABLE
(PRGCANR)
Latch Match Circuit
265
A
Cancel Fuse Circuit
263
CANRED
Address
Fusebank Enable Circuit
261
EFEN
Redundant Fusematch Circuit
255
MATCH
(RBmPHn)
To Redundant Element Driver

FIGURE 236

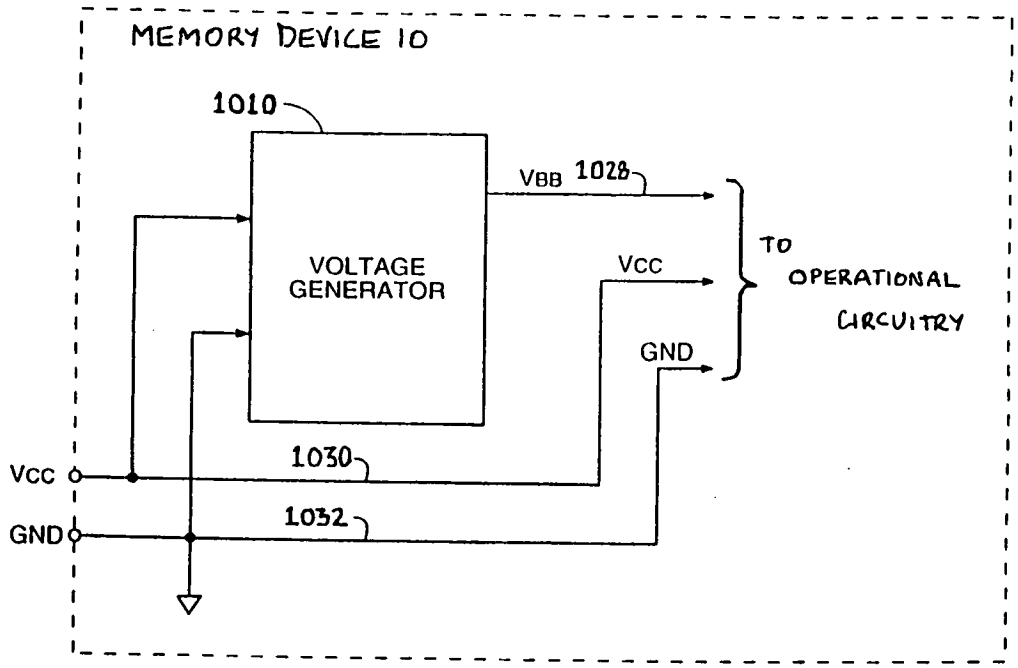

MEMORY DEVICE 10
1010
VOLTAGE GENERATOR
VBB
1028
Vcc
GND
TO OPERATIONAL CIRCUITRY
1030
1032
Vcc
GND

FIGURE 237

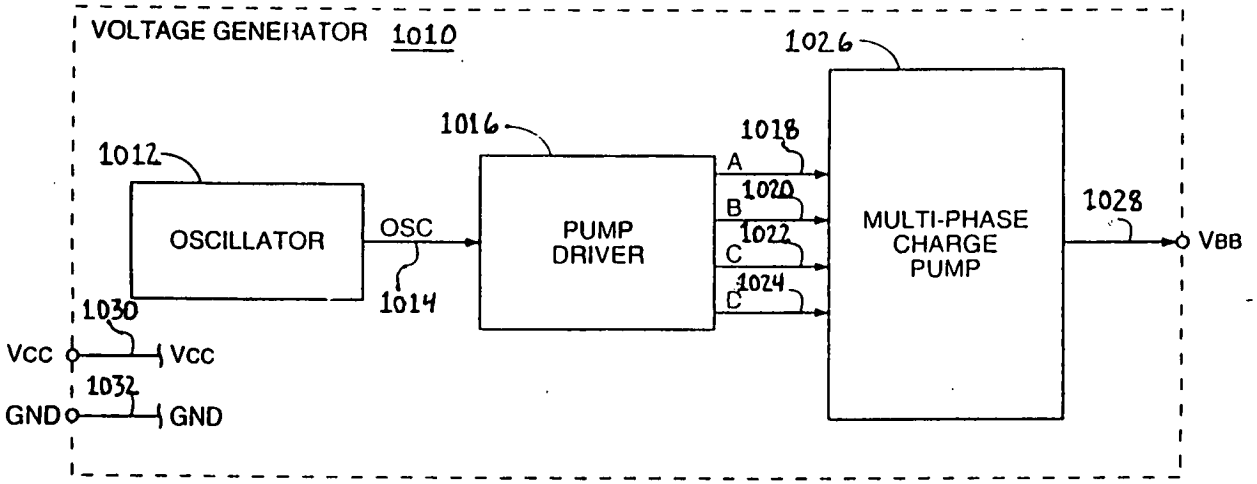

VOLTAGE GENERATOR 1010
1026
1016
1018
1012
A
1020
B
1022
C
1024
D
OSCILLATOR
OSC
1014
PUMP DRIVER
MULTI-PHASE CHARGE PUMP
1028
VBB
1030
VCC
VCC
1032
GND
GND

FIGURE 238

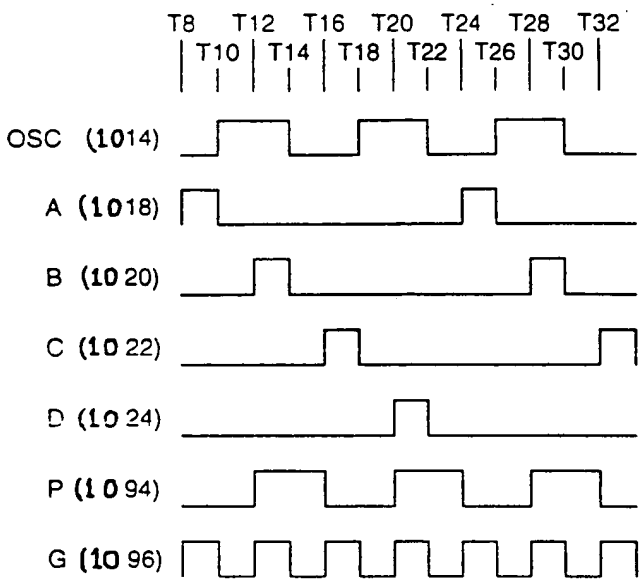

T8 T12 T16 T20 T24 T28 T32
T10 T14 T18 T22 T26 T30
OSC (1014)
A (1018)
B (1020)
C (1022)
D (1024)
P (1094)
G (1096)

FIGURE 239

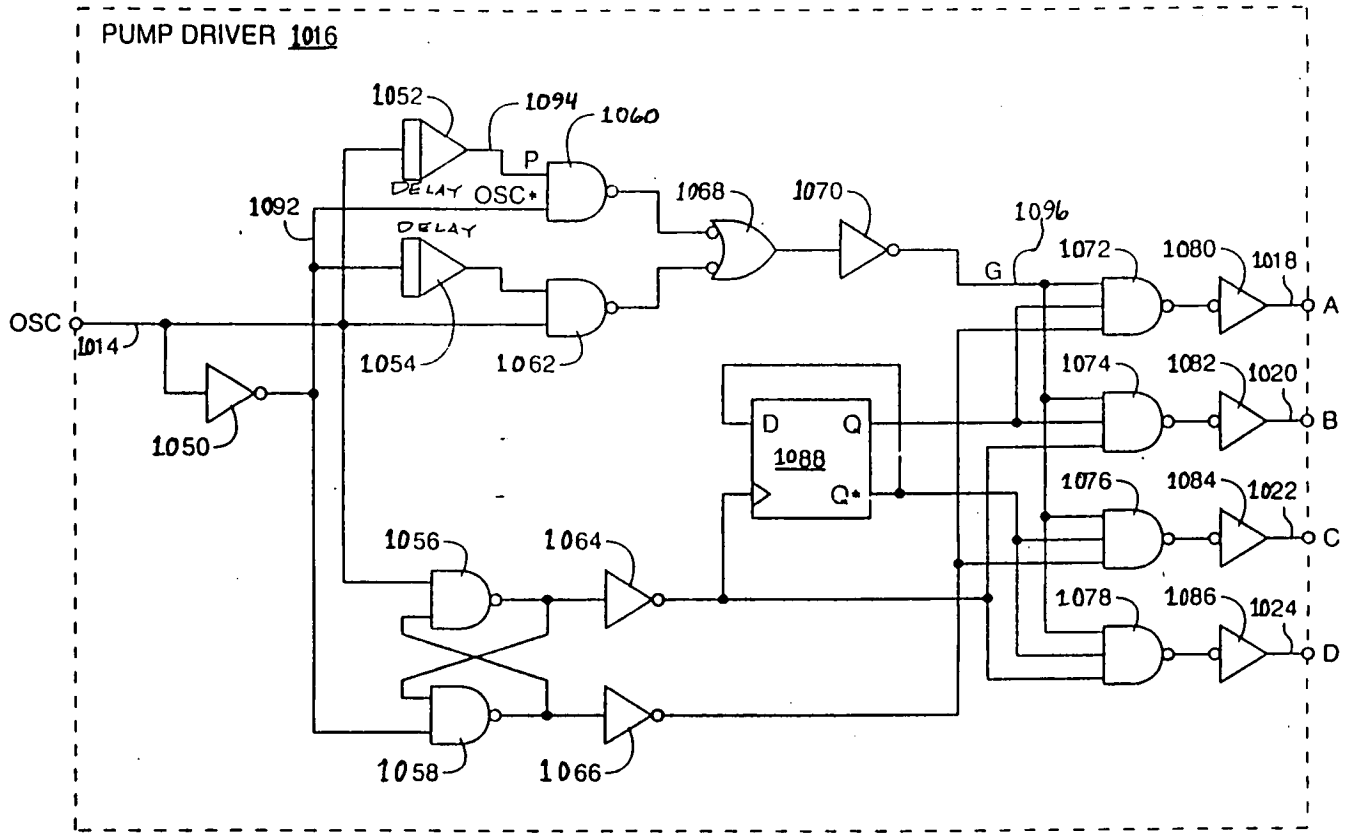

PUMP DRIVER 1016
1052
1094
1060
P
DELAY
OSC*
1092
DELAY
1068
1070
1096
G
1072
1080
1018
A
OSC
1014
1054
1062
1074
1082
1020
B
1050
D
Q
1088
Q*
1076
1084
1022
C
1056
1064
1078
1086
1024
D
1058
1066

FIGURE 240

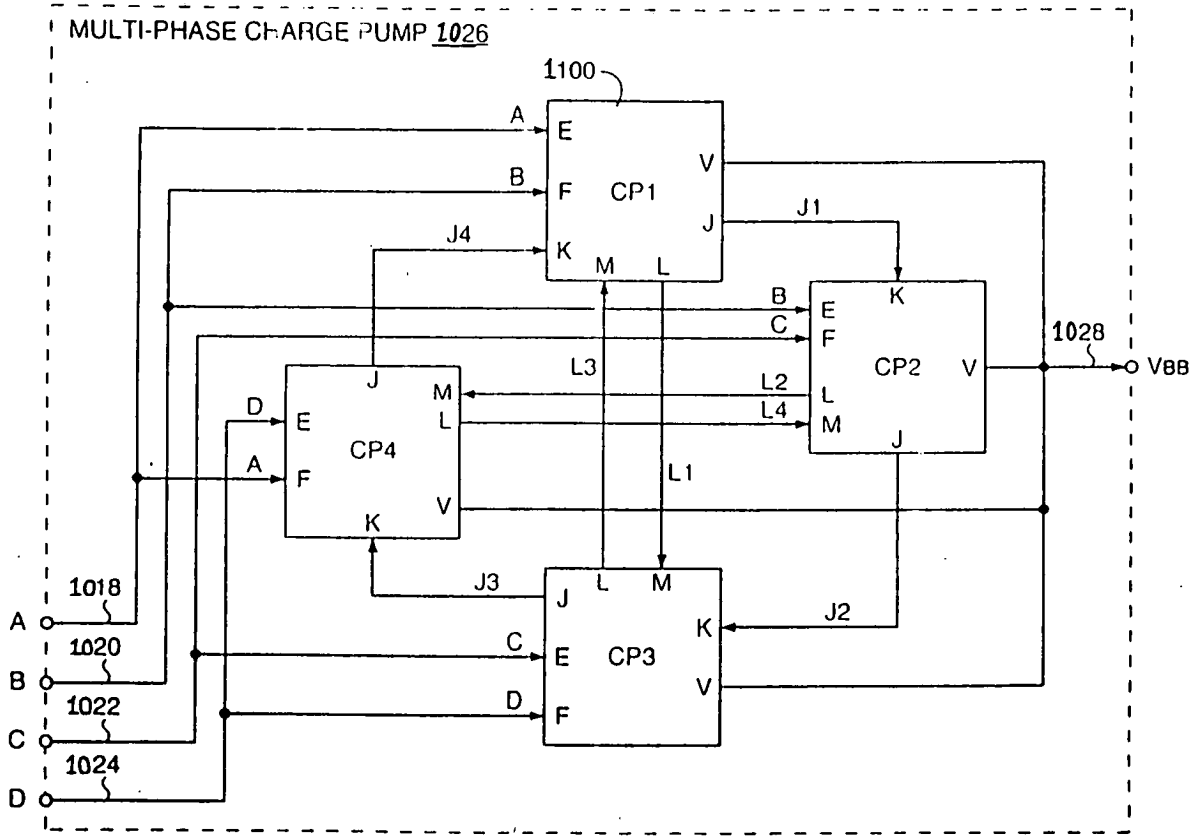

MULTI-PHASE CHARGE PUMP 1026
1100
CP1
CP2
CP3
CP4
A
B
C
D
E
F
K
V
J
M
L
J1
J2
J3
J4
L1
L2
L3
L4
1018
1020
1022
1024
1028
VBB

FIGURE 241

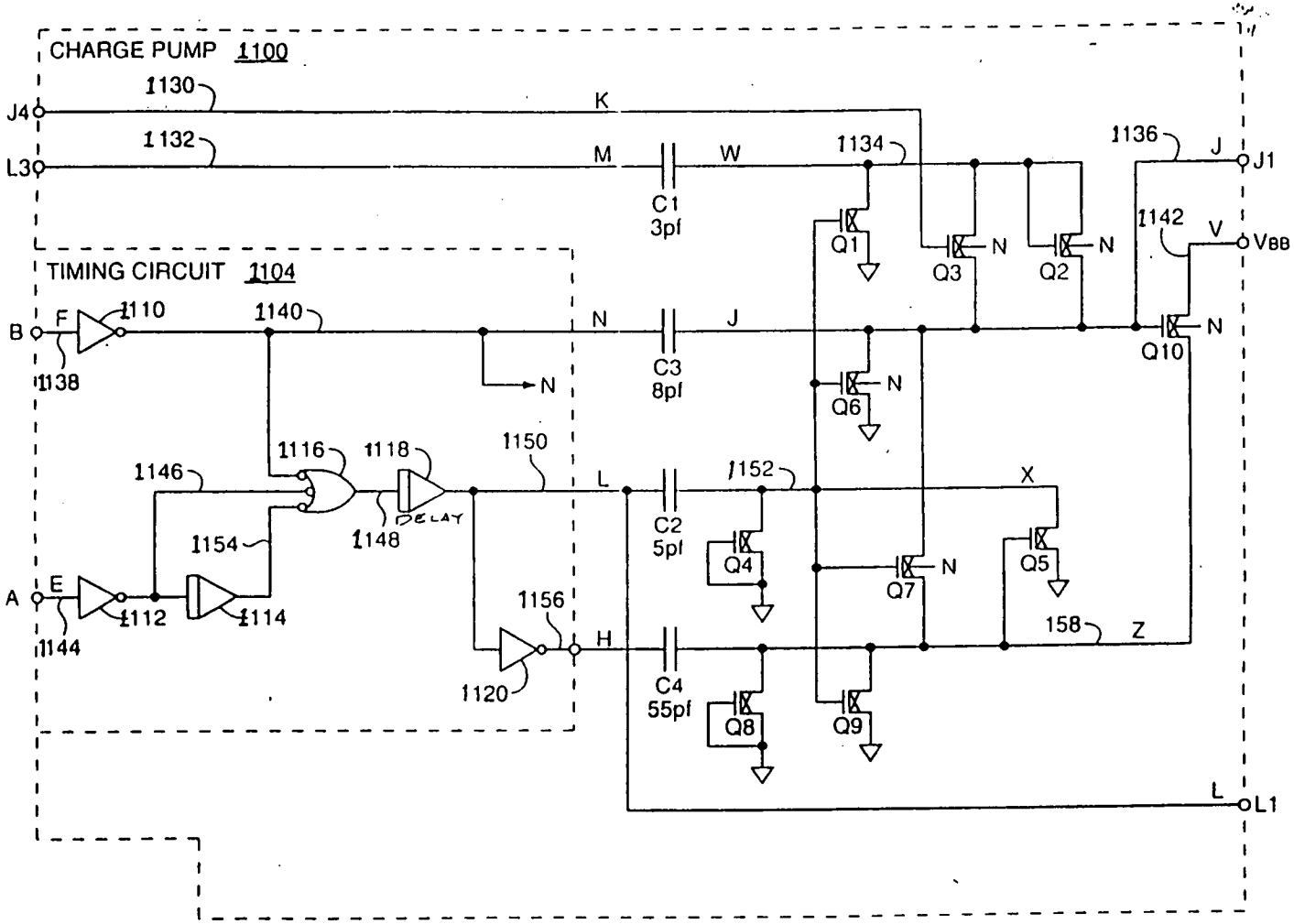

CHARGE PUMP 1100
TIMING CIRCUIT 1104
J4
L3
B
A
1130
1132
1138
1144
1110
1112
1114
1140
1146
1154
1116
1118
1148
DELAY
1150
1120
1156
K
M
W
C1
3pf
N
J
C3
8pf
L
C2
5pf
H
C4
55pf
1134
1152
Q1
Q3
Q2
Q6
Q4
Q7
Q5
Q8
Q9
X
Z
158
1136
J
J1
1142
V
VBB
Q10
L
L1

FIGURE 242

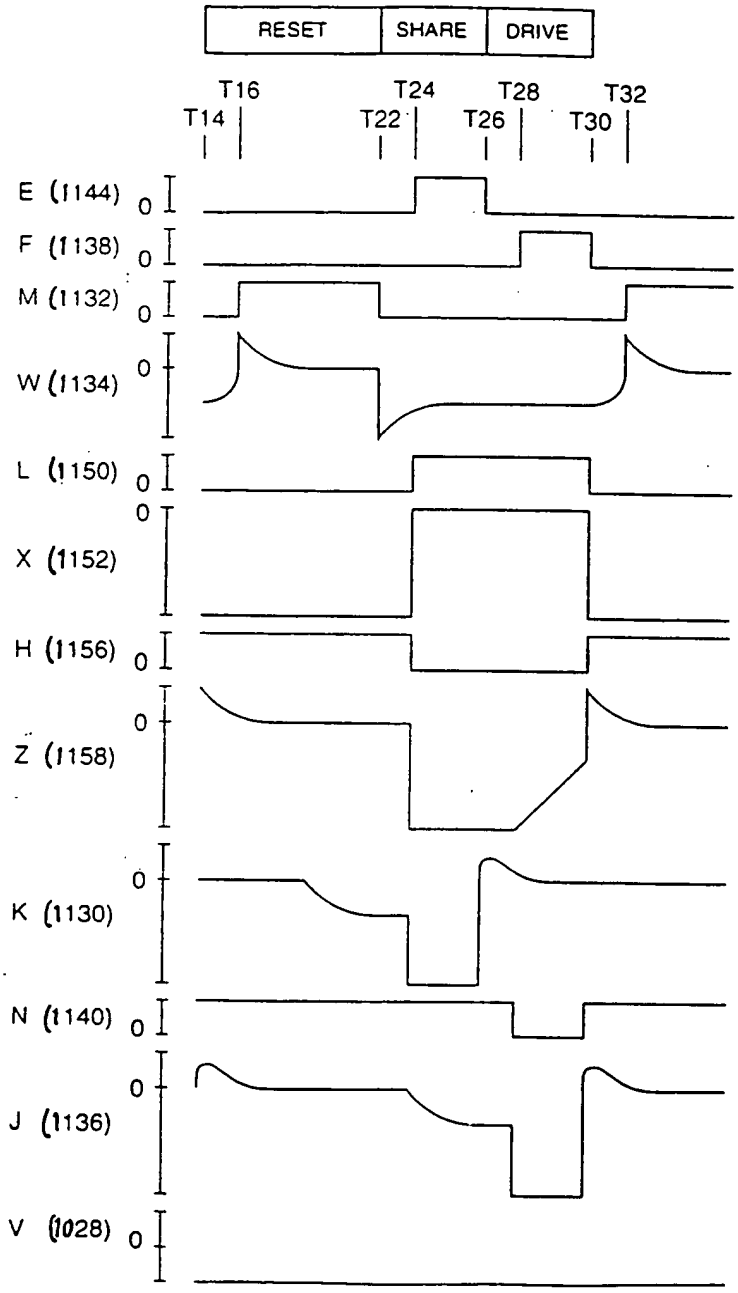

RESET
SHARE
DRIVE
T14
T16
T22
T24
T26
T28
T30
T32
E (1144)
F (1138)
M (1132)
W (1134)
L (1150)
X (1152)
H (1156)
Z (1158)
K (1130)
N (1140)
J (1136)
V (1028)
0

FIGURE 243

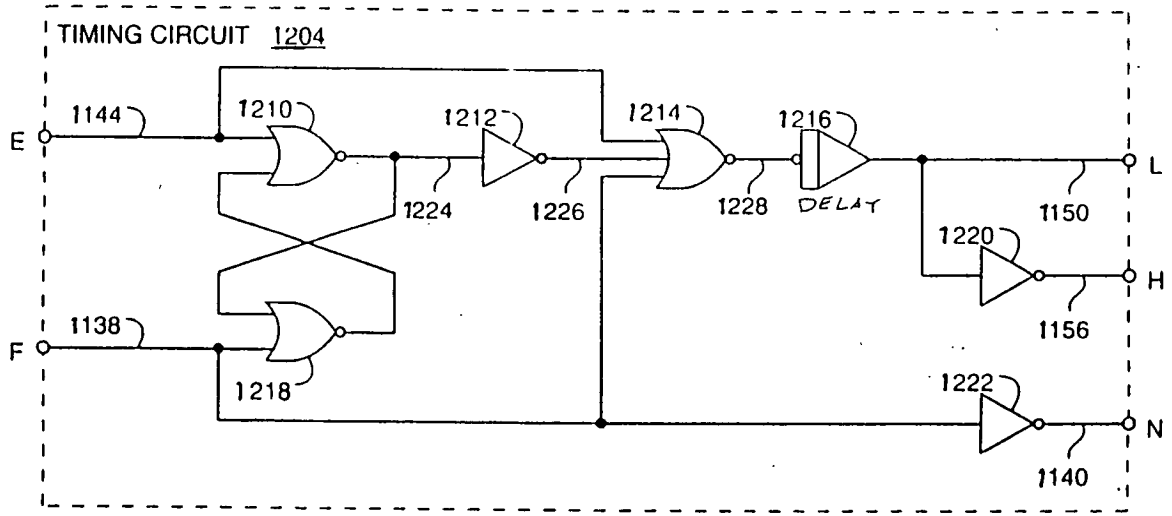

TIMING CIRCUIT 1204
E
F
1144
1138
1210
1212
1214
1216
1218
1220
1222
1224
1226
1228
DELAY
1150
1156
1140
L
H
N

FIGURE 244

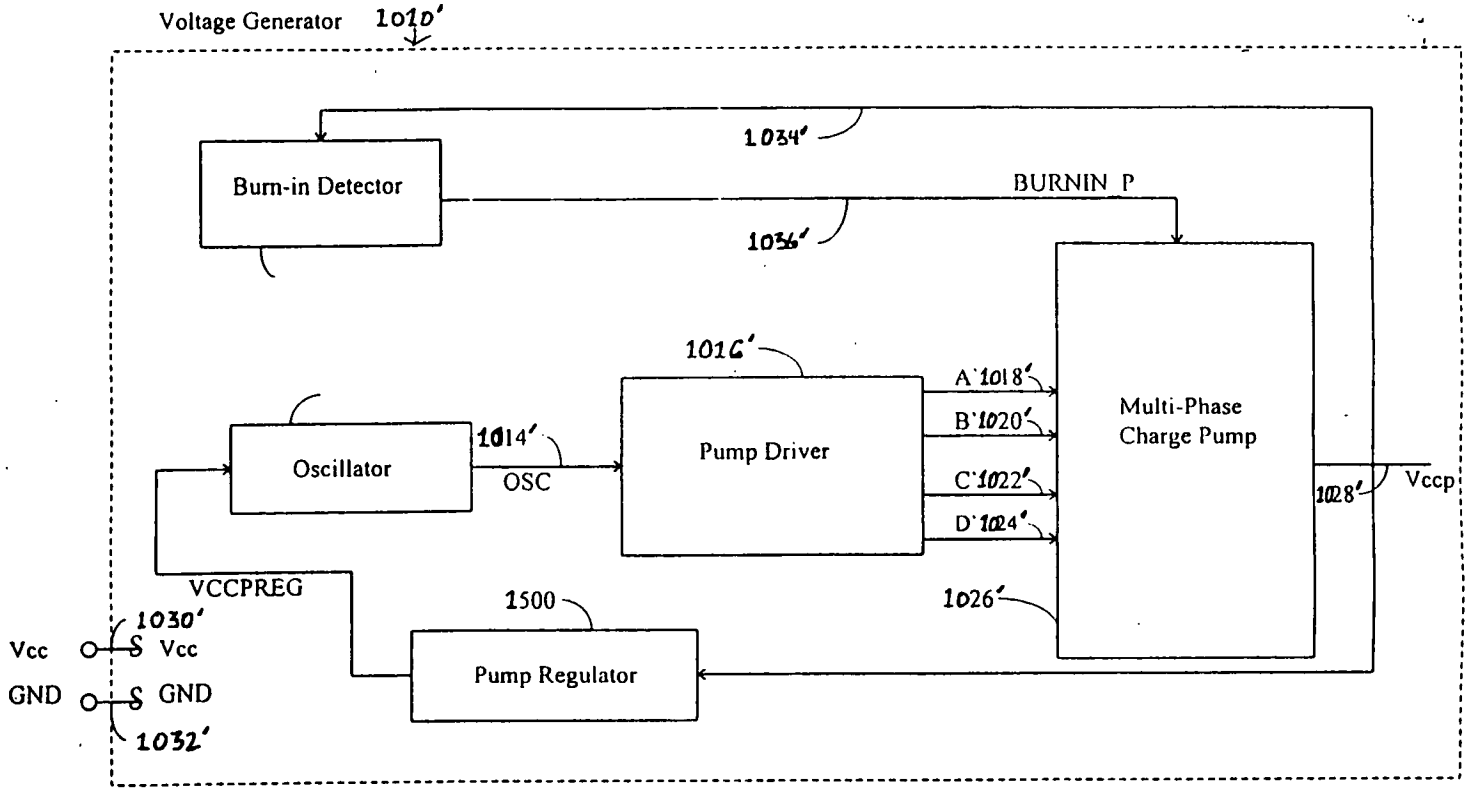

Voltage Generator 1010'
1034'
Burn-in Detector
BURNIN_P
1036'
1016'
A 1018'
B 1020'
C 1022'
D 1024'
Multi-Phase Charge Pump
1028'
Vccp
Oscillator
1014'
OSC
Pump Driver
VCCPREG
1500
1026'
1030'
Vcc
Vcc
GND
GND
1032'
Pump Regulator

FIGURE 245

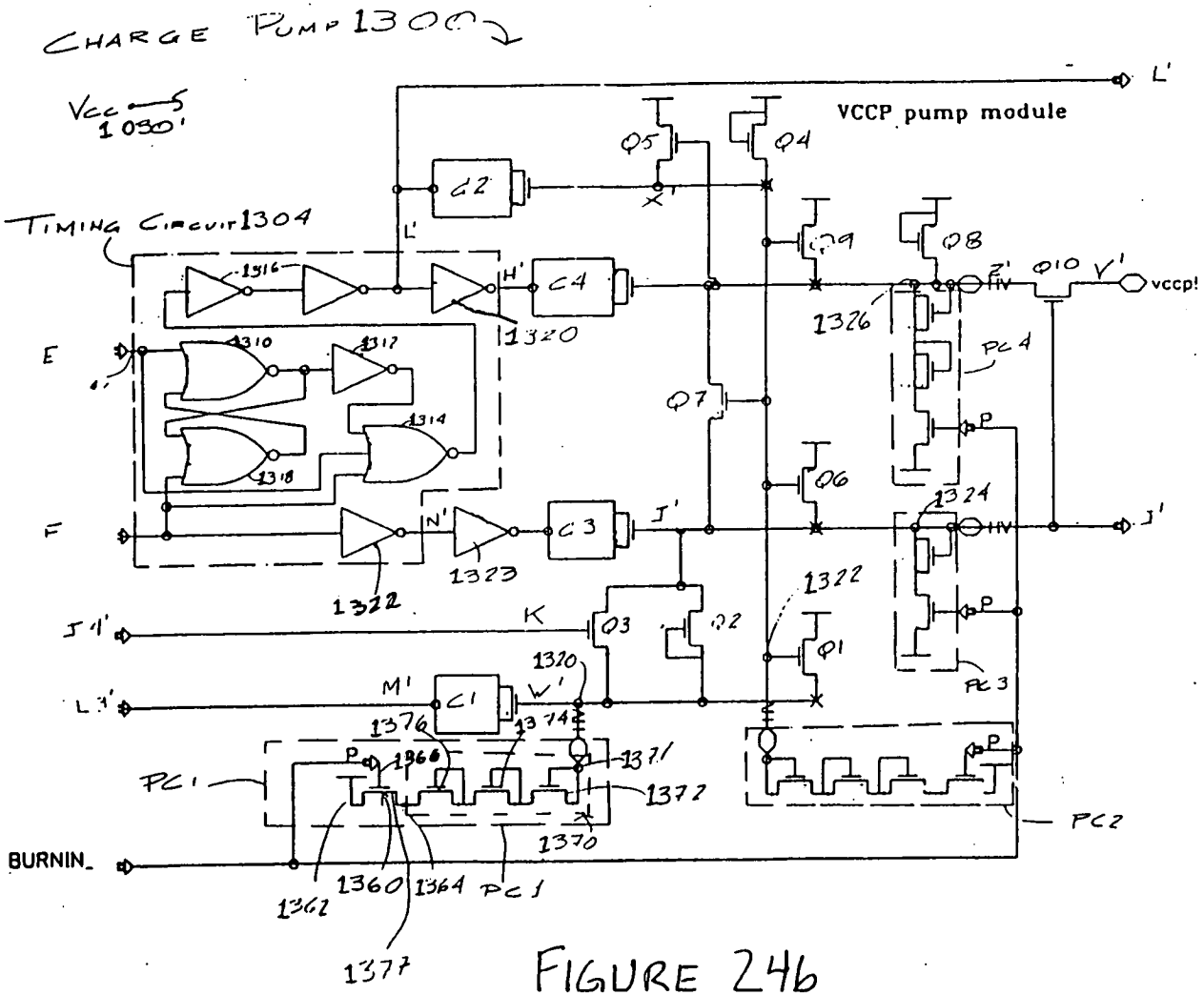

CHARGE PUMP 1300
Vcc
1030'
TIMING CIRCUIT 1304
VCCP pump module
L'
H'
N'
J'
K
M'
V'
E
F
J1'
L1'
C1
C2
C3
C4
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
1310
1312
1314
1316
1318
1320
1322
1323
1324
1326
1360
1362
1364
1366
1370
1371
1372
1374
1376
1377
PC1
PC2
PC3
PC4
P
BURNIN_
vccp!

FIGURE 246

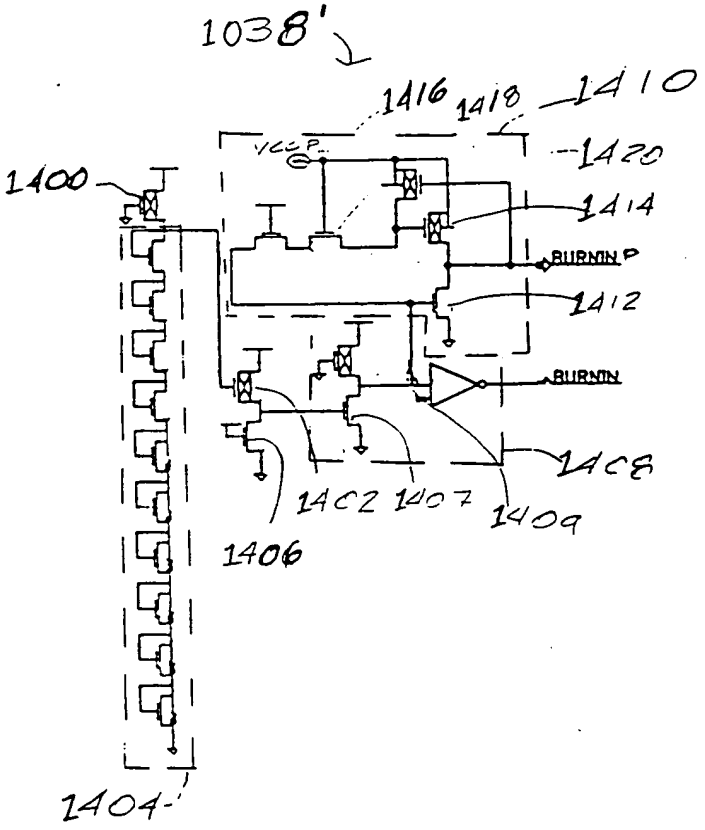

1038'
1416
1418
1410
1420
1400
1414
BURNIN P
1412
BURNIN
1408
1402
1407
1409
1406
1404

FIGURE 247

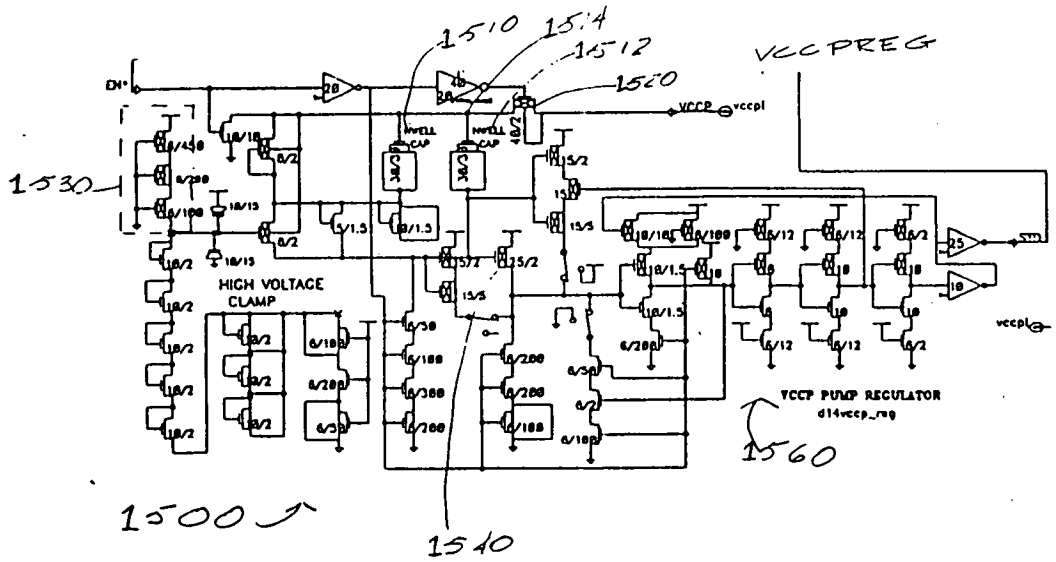

1510
1514
1512
1520
VCCPREG
VCCP
vccpl
1530
HIGH VOLTAGE
CLAMP
VCCP PUMP REGULATOR
d14vccp_reg
1560
1500
1540

FIGURE 248